

Improved Power Budget in an 8×8 Lossless SOA-based Photonic Switch in InP Platform

Hassan Rahbardar Mojaver¹, Kin-Wai Leong², Valery Tolstikhin³, Odile Liboiron-Ladouceur¹

¹Department of Electrical and Computer Engineering, McGill University, 3480 University Street, Montreal, Quebec, Canada H3A 0E9.

²Rockport Networks, 515 Legget Drive, Suite 600, Ottawa, ON, Canada K2K 3G4

³Intigent, Inc., 555 Legget Drive, Suite 304, Ottawa, ON, Canada K2K 2X3

hassan.rahbardarmojaver@mcgill.ca; kleong@rockportnetworks.com; valery.tolstikhin@intigent.com; odile@ieee.org

Abstract: A design for an 8×8 SOA-based optical switch in InP is experimentally demonstrated at 1310 nm. In this design the on-chip shuffle network loss is reduced by 11 dB.

1. Introduction

Photonic integration in InP enables for optical circuits with a variety of components, both passive and active, to be monolithically integrated onto one substrate. Among the latter there are electro-optical components with an on-chip gain, such as a semiconductor optical amplifier (SOA), which favorably distinguish InP based photonic integrated circuits (PICs) from their silica or silicon counterparts. SOA-based optical switches (OS's) in InP offer high ON/OFF extinction ratio at short reconfiguration time and, by benefiting from the on-chip optical gain, they can be made lossless. Loss neutral (i.e., lossless) OS allows for scalability and multiple input multiple output (MIMO) switch architectures not feasible otherwise [1], thereby attracting a lot of attention to InP based OS PICs as a perspective approach to next generation switch fabrics [2].

This paper reports on the lossless operation of an 8×8 SOA-based OS in InP as an example of such an approach. A monolithic PIC comprises 48 SOAs configured in three cascaded stages, each acting as an ON-OFF gate. The on-chip shuffle network loss is 32.9 dB, which is 11 dB less than that previously reported for an 8×8 SOA based InP switch [2]. Savings in the optical power budget reduce the required SOA gain, and, consequently, alleviates an impact of the amplified spontaneous emission (ASE) noise. The three SOAs in the datapath provide 35.9 dB of the optical gain, which is enough to compensate for both on-chip and fiber coupling loss. With the error-free payload transmission for all the 64 input to output paths and lossless operation with only 0.9 dB power penalty at 10 Gbps, the 8×8 OS is amongst the best of ever reported InP based switches of that kind.

2. Design and Fabrication

The design of the 8×8 OS in Banyan architecture configuration comprises twelve 2×2 SOA-based switch building blocks arranged in three cascaded stages (Fig. 1 (a)). Each 2×2 block features two 3 dB splitters at the inputs connected to the two pairs of SOAs. Each SOA acts as a gate switch by amplifying and absorbing the optical signal in the ON-state and OFF-state, respectively. Two combiners at the outputs of the SOA gates combine the optical signals. The SOAs in the first and second stages are identical each with the 11 dB of net gain. The third stage SOA is longer providing 13.9 dB of gain. On-chip optical power meters (OPMs) are inserted for monitoring and control

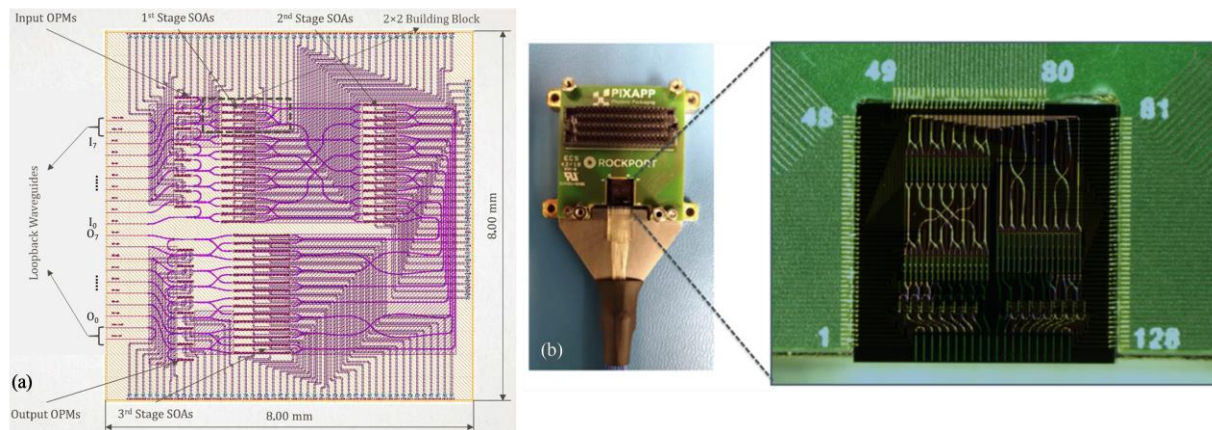


Fig. 1. (a) Layout of the 8-port OS, (b) image of the packaged OS.

applications. Each optical port is equipped with an on-chip spot-size converter (SSC) for an efficient and displacement tolerant coupling to cleaved single-mode fiber.

The InP PIC was designed and fabricated, on a commercial order from Rockport Networks, by a Consortium of Integent, VLC Photonics, and Global Communication Semiconductors, based on their proprietary regrowth-free taper-assisted vertical integration (TAVI) platform [3]. Within this platform, functional waveguides are vertically stacked in an epitaxial structure, grown in one growth run, and evanescent-field coupled to each other. The OS PIC has three such functional waveguides, top to bottom: active (bearing SOAs), passive (providing on-chip connectivity), and coupling (easing the off-chip connectivity). Controllable vertical transmission between functional waveguides, assisted by lateral tapering, in a combination with a rich library of the passive building blocks allows for a scalability of the base element of the PIC— 2×2 gate switch—into a sophisticated switch fabric. The $8 \text{ mm} \times 8 \text{ mm}$ PIC was mounted on a printed circuit board (PCB). Shown in Fig. 1 (b) are the snapshot of as fabricated 8×8 OS and photograph of its package.

3. Characterization

Continuous wave (CW) experimental measurements assess the OS lossless operation. When all three SOAs in with the datapath are biased at 70 mA or higher, the OS exhibits lossless operation at 1310 nm. The output OSNR with 0.1 nm bandwidth resolution is greater than 30 dB for input power higher than -5 dBm . The SOAs in each stage provide at least 23.6 dB of extinction ratio. Figure 2 demonstrates the error-free results (BER of 10^{-12}) for 10 Gbps nonreturn-to-zero (NRZ) PRBS-31 payload transmission over all the 64 available input to output optical datapaths. The signal-to-noise ratio (SNR) is indicated for each recorded eye diagram. The SNR is between 5.5 and 8.5. The smaller peak-to-peak value observed in the eye diagram of $I_2\text{-}O_3$ is related to the higher shuffling loss observed in this path. The optical input power to the chip is set to -5 dBm for all cases. The SOA's bias current of each stage achieves lossless operation with the largest SNR. Figure 2 reveals the excellent operation of all 48 SOAs and 16 input/output ports. The power penalty at -5 dBm input power is 1.3 dB. The power penalty decreases to 0.9 dB for -2 dBm input power (Fig. 3). This is the maximum available input power considering our testbed limitations. The power penalty increases with decreasing the input power as the effect of ASE noise becomes more significant.

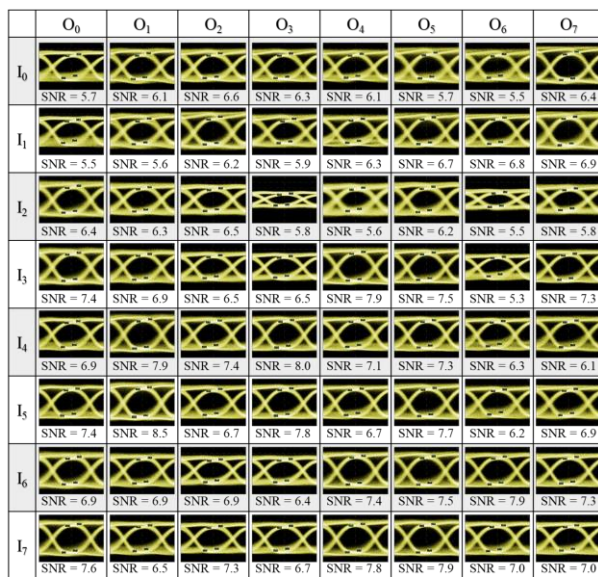


Fig. 2. Eye diagrams for 10 Gbps payload transmission over all 64 channels of the OS.

4. References

- [1] T. Kirihaara et al., "Lossless and low-crosstalk characteristics in an InP-based 4/spl times/4 optical switch with integrated single-stage optical amplifiers," *IEEE Photonics Technology Letters*, vol. 6, no. 2, pp. 218–221, Feb. 1994.
- [2] Q. Cheng et al., "The feasibility of building a 64×64 port count SOA-based optical switch," *2015 International Conference on Photonics in Switching*, pp. 199–201, 2015.
- [3] <https://www.integent.com>

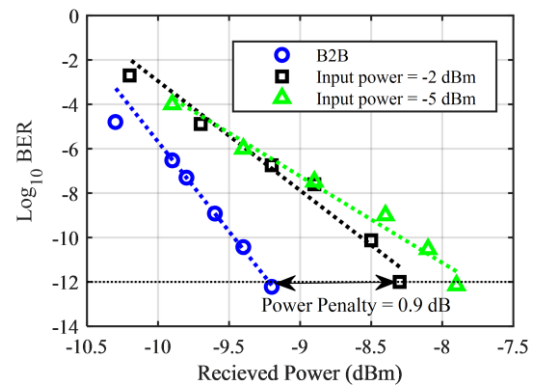


Fig. 3. BER as a function of received optical power