

Scalable SOA-Based Lossless Photonic Switch in InP Platform

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Abstract— Lossless operation of a 4×4 semiconductor optical amplifier based InP integrated photonic switch is demonstrated with performance leading to a scalable network solution. The switch maintains an optical signal-to-noise ratio of 44 dB with 0.9 dB power penalty at 25 Gbps payload transmission.

Keywords— Optical switches, photonic integrated circuits, semiconductor optical amplifiers, indium phosphide.

I. INTRODUCTION

The ever-increasing growth of internet traffic calls for higher capacity and more energy-efficient data centers [1]. While electronic switches suffer from high power consumption and latency, optical switches (OS's) may be an attractive solution, especially given that interconnects in modern data centers are already optical [2]. While most data center applications requires high radix and high input/output port count OS's, their practical implementation is limited by the insertion loss and power penalty. Development of the lossless OS's allows to overcome such a limitation, thereby providing a way for building high-scale OS fabrics [3].

Here, we report a scalable lossless 4×4 Banyan OS in InP, based on ON-OFF switching of semiconductor optical amplifier (SOA). SOAs, acting as switching gates, provide 26 dB of net optical gain in the ON state, which is enough for compensation for the insertion loss. The lossless OS maintains high optical signal-to-noise ratio (OSNR) of 44 dB, allows for 25 Gbps nonreturn-to-zero (NRZ)-PRBS 31 payload transmission with the power penalty of 0.9 dB, and can be scaled up to the extend defined by the accumulated power penalty.

II. DESIGN AND FABRICATION

The design of the 4×4 InP OS comprises four 2×2 SOA-based switch building blocks (Fig. 1). Each 2×2 block features two 3-dB Y-junction splitters at the inputs connected to the two pairs of 550 μm long SOAs. Each SOA acts as a gate switch by amplifying and absorbing the optical payload signal in the ON-state and OFF-state, respectively. Two combiners at the outputs of the SOA gates combine the optical signals. The SOAs in the first and second stages are identical with an output saturation

power of 10 dBm and noise figure (NF) of 6 dB. A 1×2 splitter taps 15% of the optical signal at the output of the second stage SOAs to waveguide photodiodes (WPD) for on-chip power monitoring and control applications. The chosen Banyan architecture provides a simpler structure with a lower number of switching elements and fewer waveguide crossings. The input and output ports have tapered waveguides with a mode field dimensions of 2.8 μm and 0.96 μm in lateral and vertical dimensions, respectively. Table I summarizes the expected loss and gain of the active and passive elements. The front and back facets of the input and output ports are coated to reduce the reflectivity below -30 dB. The OS chips were fabricated via commercial multi-project wafer run at SMART Photonics [4], with the layout design provided by VLC Photonics [5].

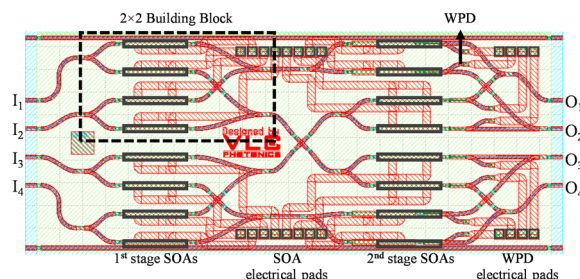


Fig. 1. Layout of the designed 4×4 SOA-based OS.

TABLE I
 LOSS/GAIN DESIGN VALUES

Switch parameters	Value
Input fiber array coupling loss	-3.0 dB
End-to-end on-chip loss	-19.0 to -20.0 dB
First stage SOA net gain	+13.0 dB
Second stage SOA net gain	+13.0 dB
Output fiber array coupling loss	-3.0 dB

III. EXPERIMENTAL VALIDATION

A set of experimental measurements validates the lossless operation of the fabricated 4×4 InP OS. To investigate the optimum gain setting of this multistage switch, Fig. 2 presents the fiber-to-fiber OS loss measured as a function of the first and second stages SOAs' bias current (I_{SOA1} and I_{SOA2}). The fiber-to-

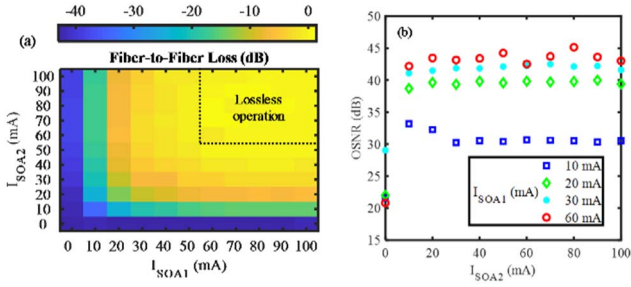


Fig. 2. (a) Fiber-to-fiber loss versus I_{SOA1} and I_{SOA2} . (b) Output OSNR versus I_{SOA2} .

fiber loss is recorded for the channel path between input I_1 and output O_4 , which represents the most lossy path (Fig. 1). The optical input power to the OS is set to 0 dBm. The OS demonstrates lossless operation for a minimum of 60 mA bias current for the first and second stage SOAs. Beyond bias current of 60 mA the SOA gain saturates. The contours of fiber-to-fiber loss versus I_{SOA1} and I_{SOA2} presented in Fig. 2 (a) show almost identical trends in fiber-to-fiber loss with respect to I_{SOA1} and I_{SOA2} . This situation leads to equal distribution of the gain and power budget between the first and the second stage SOAs. The output OSNR is measured with 0.1 nm bandwidth resolution at an input power of 0 dBm (Fig. 2(b)). With increasing the SOA's bias current, at first, the OSNR increases drastically as the SOA switches from OFF to ON-state. Then the OSNR very slightly increases up to an SOA current bias of 50 mA to 60 mA. Beyond 60 mA, the OSNR remains almost constant as the SOA gain saturates.

The experimental setup in Fig. 3(a) assesses the 25 Gbps NRZ PRBS-31 payload transmission over the OS. The measured bit error rate (BER) as a function of the average received optical power is shown in Fig. 3(b). A BER of 10^{-12} is observed for all channels at the data rate of 25 Gbps

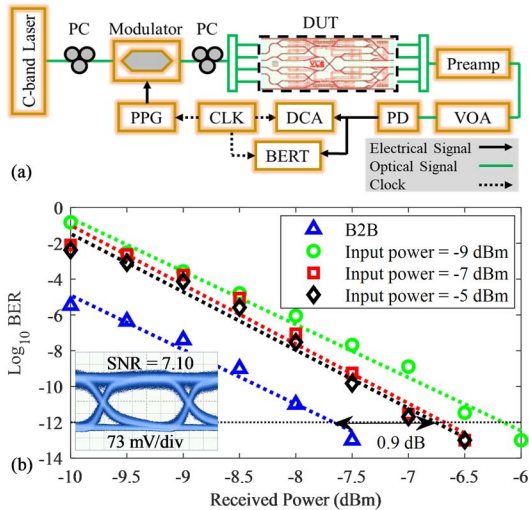


Fig. 3. (a) Experimental setup for 25 Gbps payload transmission. PC: polarization controller, DUT: device under test, VOA: variable optical attenuator, PD: photodetector, DCA: digital communication analyzer, PPG: programmable pattern generator, CLK: clock synthesizer, Preamp: preamplifier, BERT: bit error rate tester, B2B: back-to-back. The DCA and BERT are not connected at the same time to the photodetector. (b) BER as a function of received optical power.

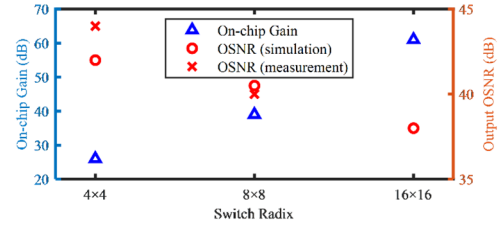


Fig. 4. On-chip gain and Output OSNR vs. OS radix.

demonstrating error-free data transmission. The power penalty at -5 dBm input power is 0.9 dB. This is the maximum available input power considering our tested limitations. The power penalty increases with decreasing the input power as the effect of amplified spontaneous emission (ASE) noise becomes more significant. The inset of Fig. 3(b) demonstrates a clear and open eye diagram at -5 dBm input power.

The SOA optical gain inevitably adds ASE noise degrading the OSNR at the output of the SOA-based OS. The ASE noise level and OSNR degradation are the main challenges in cascading the SOA-based OS's to realize a higher radix OS. Thus, the number of cascaded SOAs limits the number of channels in wavelength division multiplexing (WDM) applications [6]. Figure 4 shows the on-chip gain required for scaling to a larger radix OS. Using Lumerical's INTERCONNECT® simulation tool, we find the output OSNR (for an input power of 0 dBm) as the OS radix increases. We have validated the simulation results through experimental measurement for 4×4 and 8×8 OS's.

The optimum current bias point is 60 mA for the SOAs in both stages. At this bias level, the OS exhibits the highest OSNR and the lowest fiber-to-fiber loss while consuming the optimum energy. The voltage of the SOA at 60 mA bias current is 1.2 V; hence the OS energy consumption is 5.8 pJ/bit at 25 Gbps data rate. This is comparable to the 6 pJ/bit energy consumption reported in [7]. The energy consumption increases to 8.6 pJ/bit and 11.5 pJ/bit for the 8×8 and 16×16 OS's, respectively.

IV. SUMMARY

Lossless operation of a 4×4 SOA-based Banyan OS in InP is experimentally demonstrated. The OS generates 26 dB on-chip net gain, provided by two $550 \mu\text{m}$ SOAs biased at 60 mA, which is sufficient for compensation of its insertion loss. While operating in a lossless mode, OS consumes 5.8 pJ/bit and exhibits the OSNR greater than 44 dB.

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