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Use of a bilayer lattice-matched AlInGaN barrier for improving the channel carrier confinement of enhancement-mode AlInGaN/GaN hetero-structure field-effect transistors

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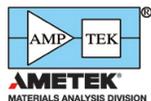
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Use of a bilayer lattice-matched AlInGaN barrier for improving the channel carrier confinement of enhancement-mode AlInGaN/GaN hetero-structure field-effect transistors

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A quaternary lattice-matched layer structure based on employing a bilayer barrier for improving the carrier confinement in the channel of enhancement-mode metal-face c-plane wurtzite AlInGaN/GaN hetero-structure field effect transistors (HFETs) is for the first time proposed. Using the commercial self-consistent Poisson-Schrödinger solver *Nextnano*, electronic properties of the proposed hetero-structure, including the sheet charge density and carrier confinement on the GaN side of the hetero-interface, are evaluated. Based on these evaluations, it is shown that while the proposed layer structure substantially improves the carrier confinement in the GaN channel layer, it also upholds the merits of employing a lattice-matched barrier towards achieving an enhancement-mode operation (i.e., in the absence of the piezoelectric effect). According to these simulations, in terms of maintaining the required positive threshold-voltage for the enhancement-mode operation, it is also shown that the proposed layer structure substantially outperforms the quaternary AlInGaN/GaN HFETs employing a thin AlN spacer layer. *Published by AIP Publishing*. [<http://dx.doi.org/10.1063/1.4989836>]

I. INTRODUCTION

Due to the presence of large polarization-induced sheet charge density at the metal-face c-plane wurtzite AlGaIn/GaN hetero-interfaces, AlGaIn/GaN hetero-structure field-effect transistors (HFETs) often manifest a negative threshold-voltage (i.e., depletion-mode operation).¹ Therefore, realization of the often needed enhancement-mode GaN-channel transistors has been proven challenging.^{2–13} Among other techniques, one of the seemingly viable solutions for realizing enhancement-mode GaN-channel HFETs is to replace the ternary AlGaIn barrier with a lattice-matched quaternary AlInGaIn layer of acceptably low spontaneous polarization mismatch to GaN.^{13,14} Accordingly, elimination of the strain (hence, the piezoelectric polarization) at the pseudomorphically grown hetero-interface has been shown to have the potential of offering these transistors a positive threshold-voltage (i.e., 0.2 V for a realistically selected barrier thickness of about 10 nm).^{13,14} Such a solution has the merit of improving the long term reliability of the device in the absence of strain at the hetero-interface. Generally speaking, variation of the metal mole-fractions of the barrier in quaternary Al_xIn_yGa_{1-x-y}N/GaN HFETs allows the engineering of both the spontaneous polarization in the quaternary barrier and the piezoelectric polarization at the hetero-interface. In turn, this can alter the polarization-induced sheet charge density at the AlInGaIn/GaN hetero-interface, leading to the ability to modify the value of the threshold-voltage of the transistor.

Although several studies have so far reported on the threshold-voltage engineering in quaternary AlInGaIn/GaN HFETs,^{10–14} quantitative assessment of the degree of carrier confinement to the GaN channel in the so-called two-

dimensional electron gas (2DEG) has remained unnoticed. Since the realization of lattice-matching between the quaternary barrier and the GaN channel has been proven to come at the unfortunate cost of reduced conduction-band discontinuity,¹⁴ leaking of the electronic wave-function of the first and especially higher subbands to the barrier seems inevitable. Such a leakage causes an increased exposure to the scattering mechanism such as alloy and interface roughness scattering, which will induce degradation in mobility and eventually the current drive of the transistor. Since in the intended enhancement-mode HFETs the transistor is often operating under a positive gate voltage, this is a problem that is much aggravated beyond the thermal-equilibrium expectations.

As a solution to the problem of carrier confinement (and also for improving the 2DEG mobility), so far a number of investigators have looked into incorporation of a very thin AlN spacer layer between the GaN channel and the AlInGaIn barrier.^{12,13,15–17} However, although thin, the incorporation of the AlN spacer is expected to result in tangible a negative shift of the threshold-voltage, caused by increasing the spontaneous polarization discontinuity and induction of strain between the channel and the spacer. Consequently, while successful in improving the conduction-band discontinuity (and the carrier confinement), the addition of the AlN spacer to the hetero-structure expectedly partially negates the gains of employing a lattice-matched barrier for achieving a positive value of threshold-voltage. Such a loss can be only compensated by taking advantage of the other techniques used in positive-shifting the threshold-voltage of GaN-channel HFETs, such as barrier-thinning,^{4,18,19} which will come at a certain cost (in this specific case, being the worsening of the gate-leakage problem via the thinned barrier).

In order to avoid the complications attributed to the use of AlN spacer, this paper looks into employing a lattice-matched

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spacer layer of inferior spontaneous polarization to AlN for achieving the required enhancement to the conduction-band discontinuity (and as a result, carrier confinement). Using the commercial self-consistent Poisson-Schrödinger solver *Nextnano*,²⁰ a quantitative assessment of the gains of employing the proposed epilayer versus AlInGaN/AlN/GaN for achieving a better confined 2DEG in enhancement-mode HFETs is presented. The accuracy of the results of *Nextnano* has been validated through comparing with the predictions of the authors' previously reported variational model.¹⁴

The basis of the HFET layer structure considered in modeling is presented in Sec. II. Section III presents the results and discussion. Section III is followed by concluding remarks.

II. DEVICE STRUCTURE

The layer structures for the HFETs which are investigated in this study are depicted in Fig. 1. As shown in this figure, the simulated pseudomorphic epitaxial layer structures were assumed to consist of a substrate, followed by a thick undoped GaN buffer/channel layer, while a 10 nm thick barrier capped by a Ni Schottky gate forms a hetero-junction to the GaN channel. Based on the composition of the barrier layer, the studied HFETs are divided into three groups.

Group 1 comprises lattice-matched quaternary $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ /GaN HFETs without a spacer layer. The barrier/spacer layers of HFETs in group 2 consist of a 9 nm thick

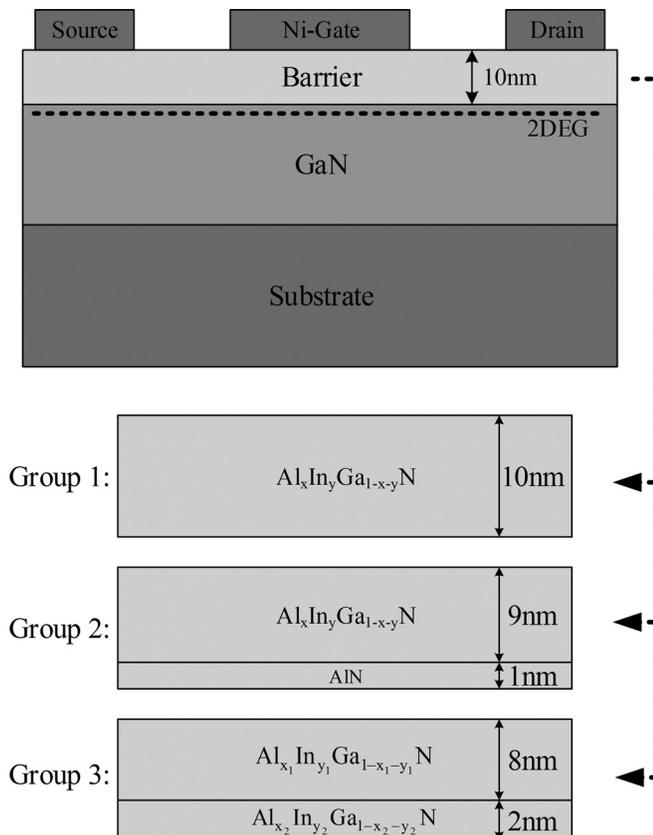


FIG. 1. Cross-sectional view of a quaternary GaN-channel HFET. Based on the composition of the barrier-layer, the studied HFETs are divided into three groups.

lattice-matched $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer and a 1 nm thick AlN spacer. Group 3 represents the proposed lattice-matched $\text{Al}_{x_1}\text{In}_{y_1}\text{Ga}_{1-x_1-y_1}\text{N}/\text{Al}_{x_2}\text{In}_{y_2}\text{Ga}_{1-x_2-y_2}\text{N}/\text{GaN}$ HFETs, in which the barrier is divided into two separate lattice-matched AlInGaN layers of different metal mole-fractions. In this latter group of HFETs, the choice of metal mole-fractions in the $\text{Al}_{x_2}\text{In}_{y_2}\text{Ga}_{1-x_2-y_2}\text{N}$ spacer layer is partially made for improving the conduction-band discontinuity (ΔE_C) to the GaN channel. While the thicknesses of the barrier and spacer layer in the first two groups were chosen in consistence with the average reported values for enhancement-mode AlInGaN/GaN HFETs (i.e., variable from 8 nm to 15 nm)^{4,13,15} the total thickness of the barrier/spacer in group 3 was taken equal to that of group 1 to allow similar device manifestation (e.g., gate depletion effect). However, in this case the alloyed nature of the spacer limits the thickness of this layer to a minimum of about 2 nm (i.e., about six times the lattice-constant).

III. RESULTS AND DISCUSSION

Figure 2 presents the variation of bandgap versus lattice constant for $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layers with indication of sheet charge density equi-contours at the $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}$ hetero-interface for different Al and In mole-fractions. Details of the calculations performed for metal-face c-plane wurtzite epilayers, which are presented in this figure, have been previously reported in Ref. 14. In this figure, shown by the black dots sitting on a straight-line indicating the lattice constant of GaN, seven different sets of metal mole-fractions for the lattice-matched quaternary $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layer are highlighted. These are the mole-fractions that are used in investigating the effect of these parameters on the carrier confinement among the three aforementioned groups of transistors. According to this figure, by reducing the Al mole-fraction, in addition to the bandgap of the barrier, the polarization-induced sheet charge density at the lattice-matched $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}$ hetero-interface decreases among the seven highlighted compositions from $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$ to $\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{GaN}$. The indicated reduction in the bandgap is associated with a reduction in

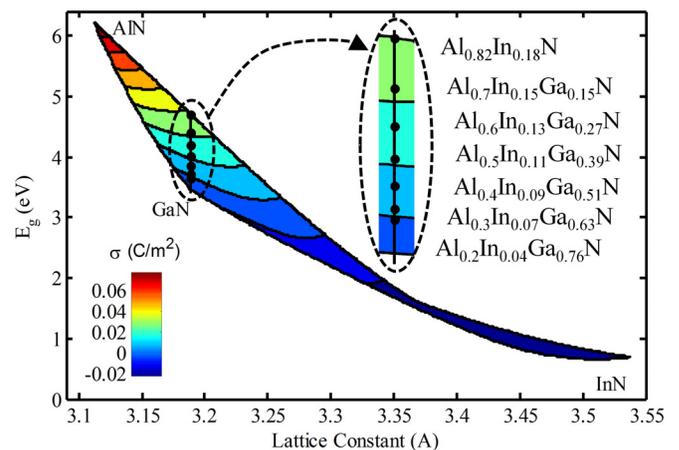


FIG. 2. Bandgap versus lattice constant for the $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ barrier-layer with indication of sheet charge density (σ) equi-contours at the $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}/\text{GaN}$ hetero-interface for the corresponding values of Al and In mole fractions. The black points indicate the position of lattice-matched $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ layers which are used in this study.

ΔE_C . As mentioned earlier, the observed co-existence of these two trends among the HFETs of group 1 results in worsening of the carrier confinement as the threshold-voltage is pushed towards positive values. As an example, Fig. 3 presents the thermal-equilibrium conduction band diagram under the gate electrode of two transistors of group 1 (i.e., two transistors with barriers of different metal mole-fractions). As shown in this figure, between $\text{Al}_{0.5}\text{In}_{0.11}\text{Ga}_{0.39}\text{N}/\text{GaN}$ and $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$, the former presents a smaller ΔE_C , while as expected from Fig. 2, a less negative threshold-voltage.

To present a quantitative assessment of carrier confinement to the GaN channel, using the commercial self-consistent solver *Nextnano*, electron concentration (n_s) as a function of the distance from the gate-metal/ $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ Schottky contact (z) was calculated among all three of the aforementioned groups of HFETs. In these calculations, n_s was evaluated using the computed wavefunctions of the first five subbands. Considering many subbands is especially consequential when the carrier confinement is poor. Figure 4 compares the form of the first five computed wavefunctions for the two examples of $\text{Al}_{0.4}\text{In}_{0.09}\text{Ga}_{0.51}\text{N}/\text{GaN}$ and $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$. Better confinement of the wavefunctions in the case of the latter HFET structure can be observed in this figure. According to these calculations, by setting the appropriate integration limits defined by the layer structure, the total per unit area electron concentration inside the gated barrier-layer $n_{s_barrier}$ and the sheet carrier concentration in the underlying GaN channel n_{s_GaN} can be assessed individually, while n_{s_total} is the total electron concentration per unit area (i.e., calculated from the Schottky contact to the bottom of GaN buffer layer). The ratio of $n_{s_barrier}$ to n_{s_GaN} offers a quantitative tool for assessing the degree of carrier spilling out of the GaN channel. In the evaluations presented here, the values of the threshold-voltage V_{th} of samples were calculated using linear extrapolation of n_{s_GaN} versus gate voltage (V_G). Figure 5 demonstrates the assessment of threshold-voltage in the specific case of a group 1 HFET. In evaluating the carrier confinement, since the value of V_{th} is varying among HFET of different layer structures and compositions,

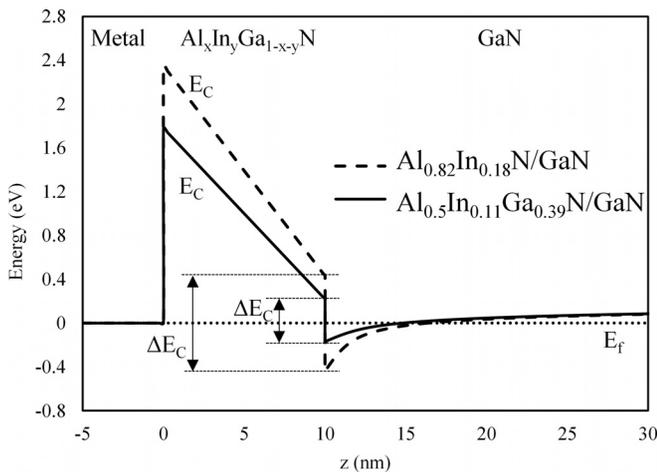


FIG. 3. Thermal-equilibrium conduction band (E_C) diagrams of Ni-gated $\text{Al}_{0.5}\text{In}_{0.11}\text{Ga}_{0.39}\text{N}/\text{GaN}$ (full line) and $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$ (dashed line) HFETs. E_f indicates the fermi-level and z is the axis normal to the hetero-interface.

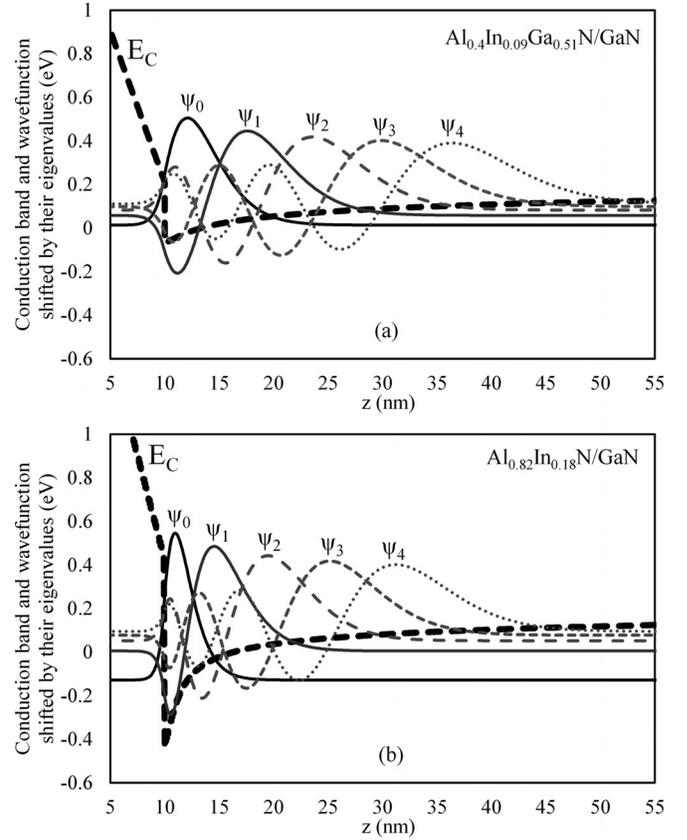


FIG. 4. Computed wavefunctions of the first five subbands ($\psi_0, \psi_1, \psi_2, \psi_3$, and ψ_4) for (a) $\text{Al}_{0.4}\text{In}_{0.09}\text{Ga}_{0.51}\text{N}/\text{GaN}$, and (b) $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$ HFETs at $V_G=0$ V. The wavefunctions are normalized to $1\text{ nm}^{-1/2}$ and shifted by their eigenvalues.

the comparisons reported in this section were made while transistors were biased at different values of V_G yielding an identical value of n_{s_GaN} .

Figure 6, as an example, compares the electron concentrations calculated for two of the group 1 HFETs, while Table I summarizes $n_{s_barrier}$, n_{s_GaN} , and n_{s_total} among the seven HFETs of this group. Based on the results presented in Fig. 6 and Table I, corresponding to a lower carrier confinement, in the transistors with smaller ΔE_C and polarization, a larger

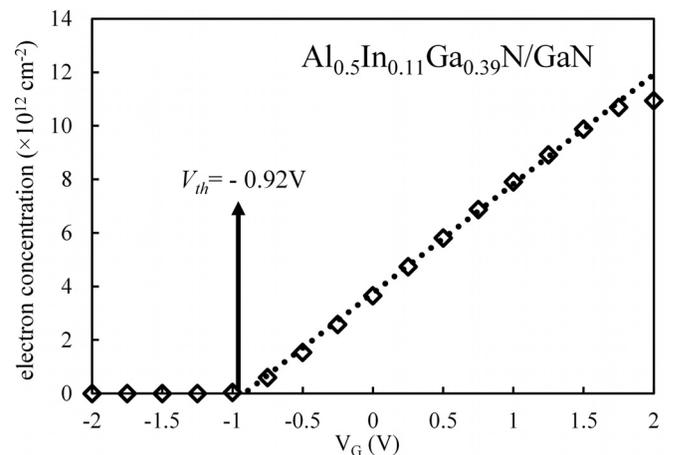


FIG. 5. Calculation of the threshold-voltage based on the linear extrapolation of n_{s_GaN} versus V_G for $\text{Al}_{0.5}\text{In}_{0.11}\text{Ga}_{0.39}\text{N}/\text{GaN}$ HFET.

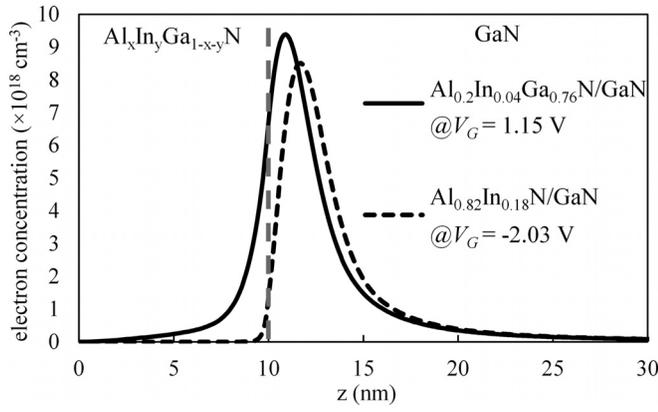


FIG. 6. Electron concentration versus z under the gate of two HFETs of group 1 (i.e., with different metal mole-fractions of the barrier-layer). Since the two HFETs manifest different values of threshold-voltage, the comparison has been made while transistors are biased at different values of V_G yielding identical values of n_{s_GaN} .

portion of carriers spill into the barrier. Among the seven explored device varieties of this group, $\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{GaN}$ with comparatively large positive V_{th} (which may be considered as a good choice for an enhancement-mode lattice-matched quaternary HFET) shows a relatively poor carrier confinement with 18.55% of the carriers residing inside the barrier at a reasonable V_G of just about 0.95 V above V_{th} .

As mentioned earlier, a common method to shift the peak of the electron concentration away from the hetero-interface (and to enhance the carrier confinement) in AlGaN/GaN HFETs is to employ an AlN spacer layer.²¹ While the use of such a spacer in the case of $\text{AlInGaN}/\text{GaN}$ HFETs has been also reported,^{12,13,15–17} as shown in Table II such a choice seems counterintuitive. Table II presents the electron concentration across different regions of the seven indicated gated epilayers of group 2. According to this table, although employing a 1 nm thick AlN spacer layer considerably

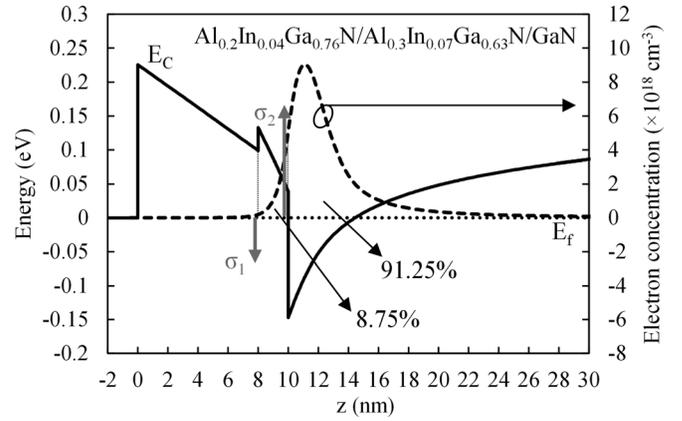


FIG. 7. Thermal-equilibrium conduction-band diagram and n_s versus z for the Ni-gated $\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{Al}_{0.3}\text{In}_{0.07}\text{Ga}_{0.63}\text{N}/\text{GaN}$. $\sigma_1 = -0.36 \mu\text{C}/\text{cm}^2$ and $\sigma_2 = 1.05 \mu\text{C}/\text{cm}^2$ are the polarization-induced sheet charge densities at $\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{Al}_{0.3}\text{In}_{0.07}\text{Ga}_{0.63}\text{N}$ and $\text{Al}_{0.3}\text{In}_{0.07}\text{Ga}_{0.63}\text{N}/\text{GaN}$ hetero-interfaces, respectively. Threshold-voltage has been calculated as +0.14 V and $n_{s_barrier}/n_{s_total}$ is 8.75% for this HFET at $V_G = 1.02$ V.

improves the carrier confinement, V_{th} of the devices of group 2 is observed to be considerably negatively shifted. This amount of shift prevents the lattice-matched $\text{AlInGaN}/\text{GaN}$ HFETs to realize an enhancement-mode operation unless employing a thinner overall barrier. Thinning of the barrier, since adding to the problem of gate leakage, is however not a very viable solution. Since compared to group 1 HFETs, group 2 HFETs manifest larger values of polarization induced sheet charge density at the hetero-interface, the collective n_{s_GaN} used in Table II is comparatively larger than the one in Table I.

Based on the above observation of the substantial impact of the largely lattice-mismatched AlN spacer layer of considerable spontaneous polarization mismatch to GaN in negating the gains of the lattice-matched epilayers for achieving enhancement-mode operation, an epilayer design relying on

TABLE I. Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 1.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm^{-2})	$n_{s_barrier}$ (cm^{-2})	n_{s_total} (cm^{-2})	$n_{s_barrier}/n_{s_total}$ (%)
$\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{GaN}$	+0.20	1.15	3.42×10^{12}	7.79×10^{11}	4.2×10^{12}	18.55
$\text{Al}_{0.3}\text{In}_{0.07}\text{Ga}_{0.63}\text{N}/\text{GaN}$	+0.02	0.92	3.42×10^{12}	3.14×10^{11}	3.74×10^{12}	8.40
$\text{Al}_{0.4}\text{In}_{0.09}\text{Ga}_{0.51}\text{N}/\text{GaN}$	-0.43	0.46	3.42×10^{12}	1.51×10^{11}	3.57×10^{12}	4.22
$\text{Al}_{0.5}\text{In}_{0.11}\text{Ga}_{0.39}\text{N}/\text{GaN}$	-0.92	-0.05	3.42×10^{12}	9.00×10^{10}	3.51×10^{12}	2.56
$\text{Al}_{0.6}\text{In}_{0.13}\text{Ga}_{0.27}\text{N}/\text{GaN}$	-1.48	-0.64	3.42×10^{12}	5.90×10^{10}	3.48×10^{12}	1.69
$\text{Al}_{0.7}\text{In}_{0.15}\text{Ga}_{0.15}\text{N}/\text{GaN}$	-2.11	-1.31	3.42×10^{12}	4.08×10^{10}	3.46×10^{12}	1.18
$\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$	-2.80	-2.03	3.42×10^{12}	2.87×10^{10}	3.45×10^{12}	0.83

TABLE II. Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 2.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm^{-2})	$n_{s_barrier}$ (cm^{-2})	n_{s_total} (cm^{-2})	$n_{s_barrier}/n_{s_total}$ (%)
$\text{Al}_{0.2}\text{In}_{0.04}\text{Ga}_{0.76}\text{N}/\text{AlN}/\text{GaN}$	-0.98	0.73	7.58×10^{12}	3.34×10^{10}	7.62×10^{12}	0.44
$\text{Al}_{0.3}\text{In}_{0.07}\text{Ga}_{0.63}\text{N}/\text{AlN}/\text{GaN}$	-1.12	0.59	7.58×10^{12}	3.27×10^{10}	7.61×10^{12}	0.43
$\text{Al}_{0.4}\text{In}_{0.09}\text{Ga}_{0.51}\text{N}/\text{AlN}/\text{GaN}$	-1.51	0.21	7.58×10^{12}	3.33×10^{10}	7.62×10^{12}	0.44
$\text{Al}_{0.5}\text{In}_{0.11}\text{Ga}_{0.39}\text{N}/\text{AlN}/\text{GaN}$	-1.98	-0.24	7.58×10^{12}	3.39×10^{10}	7.62×10^{12}	0.44
$\text{Al}_{0.6}\text{In}_{0.13}\text{Ga}_{0.27}\text{N}/\text{AlN}/\text{GaN}$	-2.45	-0.76	7.58×10^{12}	3.46×10^{10}	7.62×10^{12}	0.45
$\text{Al}_{0.7}\text{In}_{0.15}\text{Ga}_{0.15}\text{N}/\text{AlN}/\text{GaN}$	-3.03	-1.36	7.58×10^{12}	3.54×10^{10}	7.62×10^{12}	0.46
$\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{AlN}/\text{GaN}$	-3.67	-2.00	7.58×10^{12}	3.63×10^{10}	7.62×10^{12}	0.48

TABLE III. Threshold-voltage and electron concentration calculated in different parts of the gated layer structure for the HFETs of group 3.

	V_{th} (V)	V_G (V)	n_{s_GaN} (cm ⁻²)	$n_{s_barrier}$ (cm ⁻²)	n_{s_total} (cm ⁻²)	$n_{s_barrier}/n_{s_total}$ (%)
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.3} In _{0.07} Ga _{0.63} N/GaN	+0.14	1.02	3.42×10^{12}	3.28×10^{11}	3.75×10^{12}	8.75
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.4} In _{0.09} Ga _{0.51} N/GaN	+0.07	0.90	3.42×10^{12}	1.53×10^{11}	3.58×10^{12}	4.27
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.5} In _{0.11} Ga _{0.39} N/GaN	-0.05	0.78	3.42×10^{12}	9.02×10^{10}	3.51×10^{12}	2.57
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.6} In _{0.13} Ga _{0.27} N/GaN	-0.15	0.66	3.42×10^{12}	5.90×10^{10}	3.48×10^{12}	1.70
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.7} In _{0.15} Ga _{0.15} N/GaN	-0.28	0.52	3.42×10^{12}	4.08×10^{10}	3.46×10^{12}	1.18
Al _{0.2} In _{0.04} Ga _{0.76} N/Al _{0.82} In _{0.18} N/GaN	-0.41	0.38	3.42×10^{12}	2.87×10^{10}	3.45×10^{12}	0.83

the use of a lattice-matched bilayer barrier was considered (group 3). Among these epilayers, in order to achieve the best possible carrier confinement while a V_{th} compatible with the enhancement-mode operation is sustained, the metal mole-fractions of the 8 nm thick Al_{x₁}In_{y₁}Ga_{1-x₁-y₁}N barrier layer were chosen for minimization of the spontaneous polarization difference to the GaN channel, while the 2 nm thick Al_{x₂}In_{y₂}Ga_{1-x₂-y₂}N spacer layer was selected with the goal of achieving the largest possible conduction-band discontinuity to GaN. Since both AlInGaN layers are lattice-matched to GaN, no piezoelectric effect exists at the hetero-interfaces. In this design, the effect of the larger spontaneous polarization mismatch between the Al_{x₂}In_{y₂}Ga_{1-x₂-y₂}N spacer layer and GaN becomes less consequential for spacers of smaller thickness.

As an example among group 3 HFETs, Fig. 7 presents the thermal-equilibrium conduction-band diagram and n_s versus z for a gated Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N/GaN HFET. As indicated in this figure, in this layer structure two sheets of polarization-induced charge are present at the Al_{0.2}In_{0.04}Ga_{0.76}N/Al_{0.3}In_{0.07}Ga_{0.63}N and the Al_{0.3}In_{0.07}Ga_{0.63}N/GaN hetero-interfaces (σ_1 and σ_2 , respectively). σ_1 and σ_2 can be calculated as

$$\sigma_1 = P_{SP}(Al_{x_1}In_{y_1}Ga_{1-x_1-y_1}N) - P_{SP}(Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N), \quad (1)$$

$$\sigma_2 = P_{SP}(Al_{x_2}In_{y_2}Ga_{1-x_2-y_2}N) - P_{SP}(GaN), \quad (2)$$

in which $P_{SP}(Al_xIn_yGa_{1-x-y}N)$ and $P_{SP}(GaN)$ are the spontaneous polarization of the quaternary Al_xIn_yGa_{1-x-y}N barrier-layer and GaN, respectively. The foundation of the calculation framework of spontaneous polarization among quaternary layers has been previously reported in Ref. 14.

According to the strategy highlighted above, Table III summarizes V_{th} and the electron concentration in different regions of the gated epilayers of group 3 HFETs. These HFETs were considered according to the best choice of metal mole-fractions for the barrier layer among the seven points identified in Fig. 2 (i.e., $x_1 = 0.2$ and $y_1 = 0.04$). As quantitatively affirmed in Table III, in the selection of metal mole fractions of the Al_{x₂}In_{y₂}Ga_{1-x₂-y₂}N spacer layer, not only the larger ΔE_C but also the enhanced polarization-induced charge density at the Al_{x₂}In_{y₂}Ga_{1-x₂-y₂}N/GaN hetero-interface (σ_2) leads to the better carrier confinement. However, this choice also causes a negative-shift in V_{th} . Reducing the thickness of the Al_{x₂}In_{y₂}Ga_{1-x₂-y₂}N spacer layer can help with positive shifting the V_{th} , as σ_1 and σ_2 approach each other. However, thinning the spacer layer is

limited by the alloyed nature of this layer. In this study, the thickness of the spacer layer has been considered as 2 nm, which is almost six times the lattice constant.

Comparing the data presented in Tables I–III, it can be concluded that in comparison to the conventional lattice-matched Al_xIn_yGa_{1-x-y}N/GaN HFETs, employing a bilayer lattice-matched spacer/barrier offers a substantial improvement to carrier confinement in the enhancement-mode HFET (i.e., by about 10% at 1 V of gate overdrive), while imposing very little negative shift on V_{th} . The expected gain in carrier confinement by adopting the group 3 design strategy is expected to be further improved at higher gate overdrives. As a result of these observations, on the balance of the indicated factors, the proposed layer structure seems to offer the most viable solution for achieving enhancement-mode operation in the lattice-matched GaN-channel transistors. While in comparison to group 2, group 3 transistors are expected to suffer more from remote alloy scattering, the elimination of the piezo-electric effect and better confinement of electrons to the higher mobility GaN channel are expected to offer these transistors a superb current drive in the enhancement-mode operation.

IV. CONCLUSION

Based on the simulations performed using the commercial Poisson-Schrödinger solver *Nextnano*, a quaternary lattice-matched AlInGaN bilayer barrier/spacer design for GaN-channel HFETs was presented. Accordingly, it was shown that this layer structure has the possibility of offering enhancement-mode operation, while allowing good carrier confinement at substantial gate overdrives. Since the proposed barrier/spacer stack is fully lattice-matched to the GaN channel, it also allows for relieving some of the difficulties often attributed to strain relaxation and long term reliability of these polar III-Nitride hetero-structures.

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