High Radix SOA-Based Lossless Optical Switch Prototyping for 25 GBaud PAM4 Transmission in Modern Intra-datacenter Applications

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Abstract: In a development towards high-radix datacenter networks, we demonstrate 25 GBaud PAM4 transmission through a three-stage 8 × 8 SOA-based lossless optical switch, implemented as a monolithic photonic integrated circuit in indium phosphide. © 2021 The Author(s)

1. Introduction

The ever-increasing internet traffic calls for higher capacity data centers (DC's) [1]. Optical switching is considered as a promising alternative to conventional DC networks, which may increase bandwidth capacity, decrease data transfer latency, and improve energy efficiency [2]. One major challenge faced by the optical switch (OS) based DC networks is their scalability, owing to a rapid increase of the OS insertion loss and power penalty with the port count. Therefore, development of a lossless OS (LOS) with a scalable port count is crucial to scalable DC optical networks.

Previously, the integrated LOS's have been demonstrated in monolithic indium phosphide (InP) and hybrid silicon photonics (SiPh)/InP platforms [3,4]. In both cases optical loss incurred in a process of switching is compensated with optical gain provided by semiconductor optical amplifiers (SOAs). However, the optical gain comes with amplified spontaneous emission (ASE) noise and nonlinear distortion, which may compromise the payload signal integrity. Introducing additional amplitude levels in PAM4 signaling further complicates the situation by virtue of reducing the optical signal to noise ratio (OSNR). Therefore, evaluation of the PAM4 transmission performance of a high-radix LOS would be an important step towards understanding of the OS-based DC network scalability.

The switching performance of an SOA-based 1 × N broadcast and select OS using 14 GBaud (28 Gbps) PAM4 traffic has been already evaluated [5]. A power penalty of 0.8 dB at a targeted BER of 2.4×10^{-4} was reported for the 1 × 8 switch fabric. Due to the OSNR degradation caused by higher splitting loss, approximately 3 dB extra penalty occurs when scaling from 1 × 8 to 1 × 32 ports. As the IEEE 400 Gbps Ethernet Task Force standardized 25 GBaud (50 Gbps) PAM4 transmission [6], increasing the baud-rate to 25 GBaud will further increase the BER and power penalty in a high-radix OS. Here, we report the performance of the monolithically integrated 8 × 8 SOA-based LOS, experimentally studied by transmitting a 25 GBaud PAM4 payload, in conjunction with the optical network scalability.

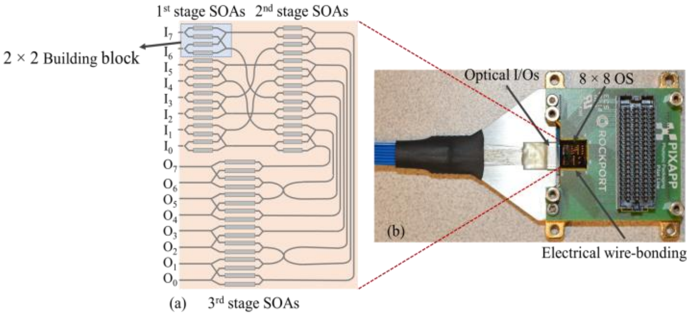

Fig. 1. (a) Schematic of the building blocks in the designed three stage SOA-based OS, (b) packaged OS prototype.

2. Design and Fabrication

The LOS photonic integrated circuit (PIC) is the same as that reported in [4]. Commissioned by Rockport Networks Inc., it was designed and prototyped by a consortium of Intengent Inc., VLC Photonics, and Global Communication

Semiconductors Inc., based on their regrowth-free taper-assisted vertical integration (TAVI) technology in InP. The LOS network is built from 2 × 2 switches organized in a Banyan configuration. Each such switch comprises a 1:2 multimode interferometer (MMI) splitter, four SOAs, and a 2:1 MMI combiner (Fig. 1-a). SOAs act as amplifiers if forward-biased (ON state) or as absorbers if reverse-biased (OFF state). The SOAs in the first and second stages are 500 µm long providing more than 16 dB gain per stage. The 3rd stage SOAs are 750 µm long to provide about 19 dB of gain. Combined, gain of three stage SOAs is sufficient for a compensation of the on-chip and coupling loss, thereby providing zero-loss fiber-to-fiber transmission. The OS package exploits edge coupling with a twenty-channel single-mode fiber array connected to the optical input and output ports equipped with on-chip spot-size converters (Fig. 1-b). The OS is mounted substrate down via an intermediate silicon spacer to a copper heat sink, and wire-bonded to a printed circuit board (PCB).

3. Transmission Experiment

CW performance of the LOS was reported in [4]. Here, we focus on 25 GBaud PAM4 payload transmission evaluation, only. The setup used in transmission experiment is depicted in Fig. 2 (a). On the transmitter side, an arbitrary waveform generator (AWG) generates a PAM4 PRBS-7 signal. The modulated input signal couples to the OS in a quasi-TE polarization, maintained by a polarization controller (PC), while current sources bias the SOAs. On the receiver side, an optical amplifier (OA), a tunable O-band optical filter with 1 nm 3-dB bandwidth, and a variable optical attenuator (VOA) are inserted between the OS output and a 40-GHz photodetector (PD). The tunable optical filter reduces the broadband ASE noise. The OA compensates for the insertion loss of the tunable optical filter (approximately 8 dB). The VOA controls the detected signal. We used a real-time oscilloscope (RTO) for analyzing the received signal.

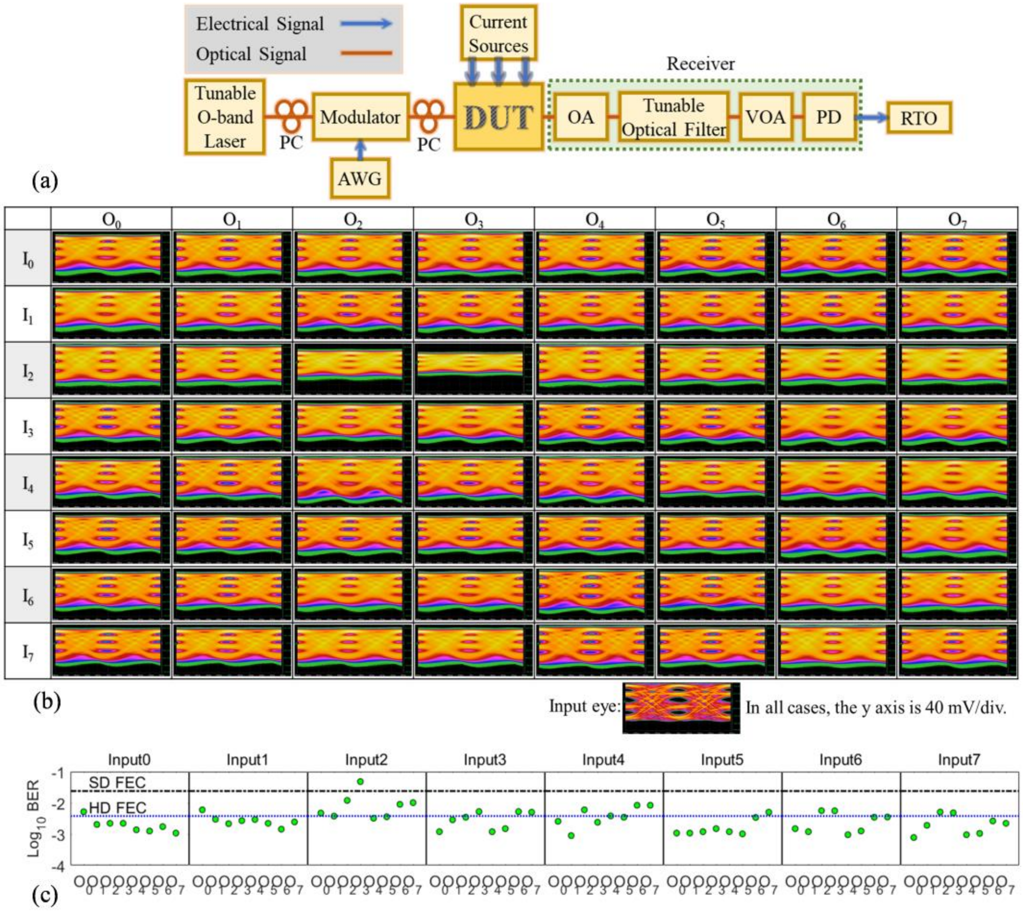

Fig. 2. (a) Experimental setup for PAM4 transmission measurements. (b) Eye diagrams for 25 Gbaud PAM4 transmission for all 64 optical paths of the 8 × 8 OS. (c) The corresponding BER for each path.

Figures 2 (b)–(c) present the eye diagrams and the corresponding BER values for all 64 optical paths, from all eight input ports (I_0 to I_7) to all eight output ports (O_0 to O_7) for 25 Gbaud PAM4 transmission. We calculated the

BER from each recorded eye diagram using the RTO. In these measurements, we set the input power to the OS at -5 dBm, while we adjust the SOA biases to obtain the lowest BER. As Fig. 2 (c) reveals, 45 out of the 64 optical paths transmit 25 Gbaud PAM4 payload with a BER below the 7% overhead hard decision forward error correction (HD-FEC) limit (*i.e.*, 3.8×10^{-3}). All the paths except I_2 to O_3 are capable of 25 Gbaud transmission with BER below 20% overhead soft decision forward error correction (SD-FEC) limit (*i.e.*, 2.4×10^{-2}). The higher error in I_2 to O_3 relates to a higher shuffling loss due to epitaxy growth issue in this first prototype aggravated by additional SOA to shallow etched waveguide coupling loss in this specific optical path [4].

Figure 3 (a) shows BER results for two selected paths: I_7 to O_0 exhibiting best performance, and optical path I_2 to O_2 with the worst performance. At 10 Gbaud, we measured a power penalty at the SD-FEC limit of 0.1 (1.4) dB for I_7 to O_0 (I_2 to O_2), and 1.7 (4.3) dB at the HD-FEC limit. The power penalty for I_7 to O_0 is 4.8 dB at KP4-FEC limit, while I_2 to O_2 cannot reach this BER limit. At 25 Gbaud, the power penalty increases to 1.4 (8.8) dB at the SD-FEC threshold BER. For I_7 to O_0, the power penalty is 4.2 dB at the HD-FEC threshold, while I_2 to O_2 cannot reach this BER limit. Results of Fig. 3 (a) reveals considerable path-dependent power penalties of OS especially at higher baud rates. As schematically illustrated in Fig. 3 (b), I_7 to O_0 includes no waveguide crossing, whereas I_2 to O_2 includes four waveguide crossings. Due to higher optical loss in the I_2 to O_2 optical path, SOAs need to be biased at higher current bias to provide larger gain. This leads to larger ASE noise in the I_2 to O_2 path, which increases the power penalty. Improvement in future designs of the 8 × 8 SOA-based OS may employ on-chip passband filters between switching stages to suppress the ASE noise. Moreover, by removing the out of band ASE noise, the bandpass optical filter prevents saturation of the second and third stage SOAs which would have led to nonlinearities.

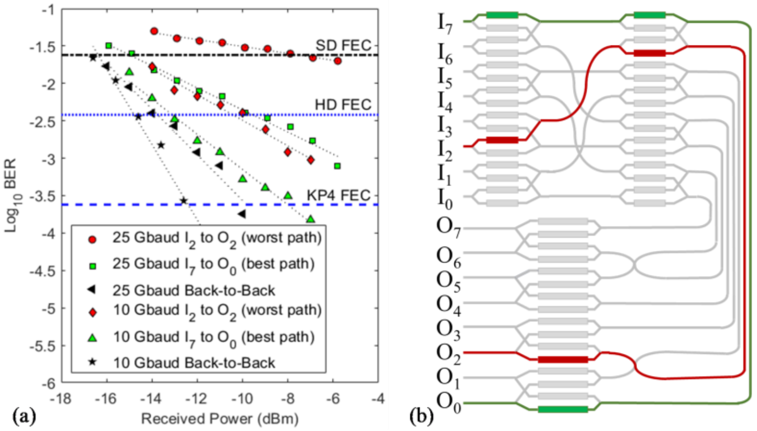

Fig. 3. (a) BER versus received optical power for I_7 to O_0 and I_2 to O_2 at 10 GBaud and 25 GBaud. (b) Schematic illustration of I_7 to O_0 and I_2 to O_2.

4. Conclusion

We presented the first experimental demonstration of 25 GBaud PAM4 optical signal transmission through a fully operational 8 × 8 SOA-based LOS with all its 64 optical paths validated. While the path-dependent power penalty is less than 1.4 dB for all data paths at 10 GBaud, it increases to 8.8 dB (worst case) at 25 GBaud, exacerbated by an excessive on-chip optical loss in this first LOS prototype.

5. Acknowledgment

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