

## 8 × 8 SOA-based optical switch with zero fiber-to-fiber insertion loss

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**The design, fabrication, and characterization of an 8 × 8 lossless optical switch, based on semiconductor optical amplifier (SOA) gates, is reported. It comprises three stages of 2 × 2 switches into an 8 × 8 Banyan switch, for a total of 48 SOAs. Three SOAs on each optical path provide gain to compensate for on-chip and fiber coupling loss, thereby making the optical switch lossless. All 64 optical paths demonstrate error-free 10 Gbps NRZ PRBS-31 transmission with at least 30 dB signal-to-noise ratio and less than 0.9 dB power penalty.** © 2020 Optical Society of America

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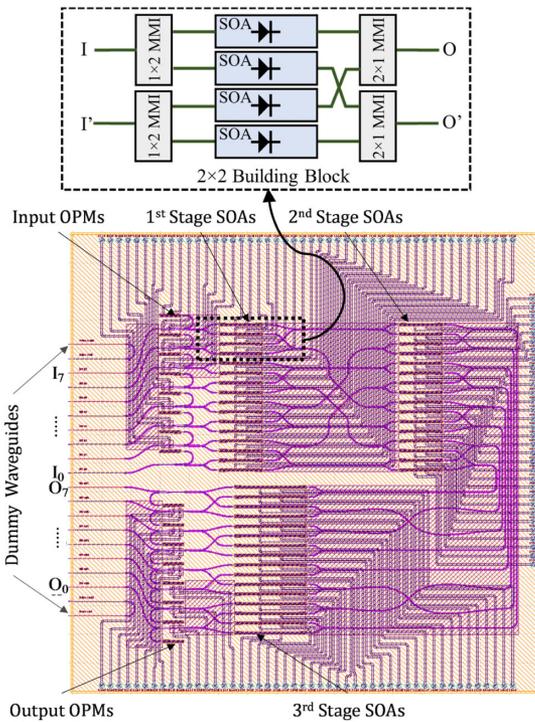
The ever-increasing growth of internet traffic requires higher capacity data centers [1]. Optical switches (OSs) are promising candidates for replacement of their electronics counterparts [2], because they offer wider bandwidth capacity, lower data transfer latency, and potentially lower power consumption [3]. However, the OS insertion loss increases with port count, whereas advanced data center applications assume high radix switches [4]. For that reason, it would be highly desirable to develop a lossless OS with a scalable port count.

Since neither insertion loss nor its scalability with the port count are avoidable, the only solution to the lossless OS is an optical gain that compensates for the optical loss. Semiconductor optical amplifiers (SOAs) in InP can provide both the off- and on-chip gain. In the first case, such SOAs are combined with a high radix but lossy OS, like those available in silicon photonics (SiP) [5], thereby providing a hybrid integrated lossless OS [6]. Whereas an interesting option for further development, hybrid integration of InP and SiP chips with multiple optical ports creates serious packaging problems [7]. In the second case, SOA by itself can be used as a base for an OS operated on the ON-OFF gate-switching principle, while also providing the gain and enabling for a monolithic integration onto one InP substrate. Indeed, such SOA-based OS photonic integrated circuits (PICs) in InP have been demonstrated [3,8],

although still with a significant fiber to fiber loss. While further increase of the on-chip gain is, probably, feasible, it is not desirable since the associated amplified spontaneous emission (ASE) noise and non-linear distortion may compromise the payload integrity [9]. The OS with lower insertion loss that would require lower on-chip gain is a preferable option.

In this Letter, we report the lossless, fiber-to-fiber, 8 × 8 SOA-based OS PIC in InP for intra-datacenter switching applications. It operates in the O-band and allows for the error-free 10 Gbps NRZ PRBS-31 transmission from any input to any output, with the optical signal-to-noise ratio (OSNR) above 30 dB and power penalty below 0.9 dB. The lossless 8 × 8 OS PIC is designed and manufactured on a commercial order for a turn-key solution from Rockport Networks by a Consortium of Integrent, VLC Photonics, and Global Communication Semiconductors, based on its proprietary regrowth-free taper-assisted vertical integration (TAVI) platform in InP (e.g., see [10]). As in other vertical integration platforms [11,12], waveguides are vertically stacked and evanescent-field coupled in an epitaxial structure grown in one growth run. The OS PIC has three functional waveguides, from top to bottom: 1) active (SOAs and optical power monitors-OPMs); 2) passive devices (MMIs, routing waveguides); 3) off-chip coupling. Active waveguide features a PIN structure with separate confinement heterostructure (SCH) and multiple-quantum well (MQW) regions. It is used as gain (under forward bias) and absorption (under reverse bias) media. Passive waveguides are shallow-etch or deep-etch ridge waveguides (SE-PWG and DE-PWG.) Off-chip coupling waveguide has spot size converters (SSCs) at the facet [13]. Lateral tapering allows for vertical transitions between functional waveguides with a smooth transition of the guided mode's effective index.

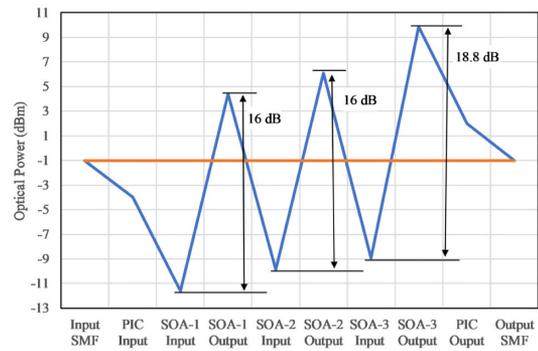
The PICs are fabricated on 4" wafers, with the epitaxial structure grown on semi-insulating Fe:InP substrates in one epitaxial growth run. The snapshot of the PIC layout and block-diagram of its key building block, the 2 × 2 SOA-based gate-switch, are provided in Fig. 1. The 8 mm × 8 mm chip comprises twelve



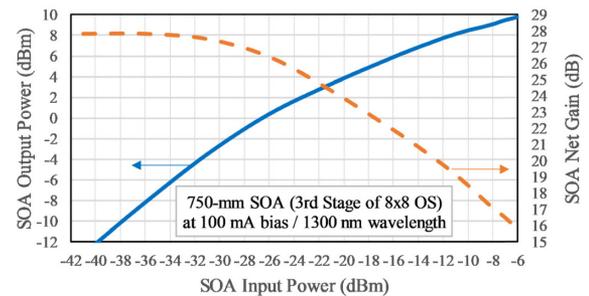
**Fig. 1.** Snapshot of the 8 × 8 OS PIC layout (bottom) and block-diagram of its key building block—SOA-based 2 × 2 gate-switch (top).

such switches, arranged in three stages. Each input of the 2 × 2 switch has a 1:2 multi-mode interferometer (MMI) splitter and each output has a 2:1 MMI combiner. Between the splitter outputs and combiner inputs there are four SOAs, each of which is working either as an amplifier (if forward-biased, ON state) or absorber (if unbiased or reverse-biased, OFF state). Transmission from input to output is only through SOA in the ON state, while SOA in the OFF state blocks the optical path. In an unsaturated regime, the extinction ratio of gate-switching increases with the bias and SOA length, which is 500 μm in the first and second stages and 750 μm in the third stage. The third stage SOA is longer to provide more gain, if necessary. The 2 × 2 switches in different stages are connected by passive waveguides, creating a shuffle network. It is designed such that eight input and eight output optical ports are at the same facet, which is anti-reflection coated. They are equipped with SSCs, formed in the coupling waveguide. Next to SSC's there are OPMs, used to monitor the incoming/outgoing optical signals. All in all, the PIC comprises 64 active devices: 48 SOAs and 16 OPMs. Each of them has two coplanar contact pads (total of 128), distributed along the non-optical facets. The chip is mounted substrate down via an intermediate silicon spacer to a copper heat sink, and wire-bonded to a printed circuit board (PCB).

The major contribution in fiber-to-fiber insertion loss comes from MMI splitters/combiners, each of which adds approximately 4 dB: 3 dB split/combine and 1 dB excess loss. Since each optical path comprises six MMIs, that is 24 dB. Then, critically important is SE-PWG to SOA and back coupling, six occurrences of which are on each optical path. In a normal course of events that would be below 1 dB per coupling, but unfortunate epitaxial growth flaw increased this loss by ~2.5 dB for a total of 15 dB per optical path. The same epitaxy issue increased



**Fig. 2.** As-fabricated and packaged 8 × 8 OS loss-gain breakdown.

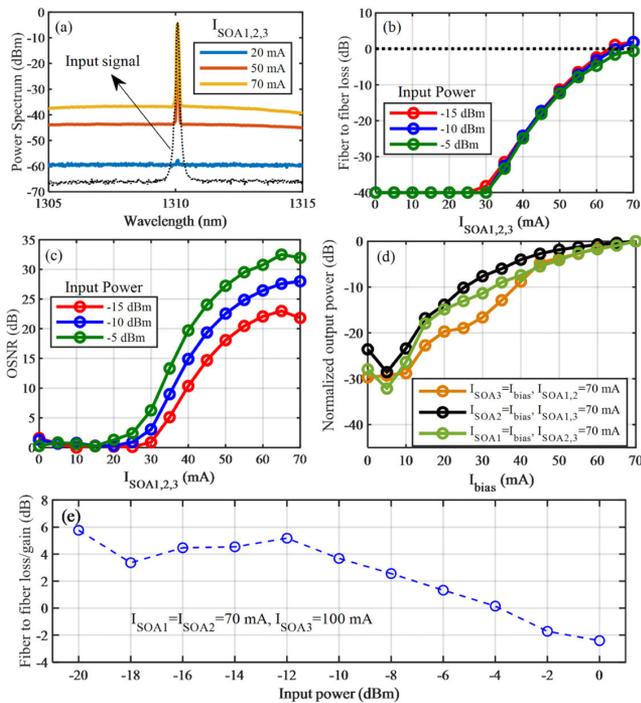


**Fig. 3.** Net gain and output power of the third stage SOA.

insertion loss on a path from single mode fiber (SMF) to SE-PWG to about 3 dB (compared to normal ~1.5 dB), adding 6 dB more. Finally, some 6 dB comes from routing that includes SE-PWG–DE-PWG coupling and DE-PWG crossing. The total fiber-to-fiber loss is approximately 51 dB. In a lossless OS, it should be compensated with an on-chip gain. Figure 2 gives an estimated loss–gain breakdown for a fiber-to-fiber optical path, based on a link budget of 50.8 dB. The noise figure (NF) is 6 dB for the first and second stage SOAs, and 8 dB for the third stage SOA. Considering the Friss formula [14], and the loss/gain values presented in Fig. 2, the total NF is 9.5 dB.

The device characterization is performed at three levels. First, the SOA gain dependence on the bias current and input power were measured in stand-alone SOAs with the same design as those in 8 × 8 OS. The set-up includes an O-band tunable laser and polarization controller (PC) at the SOA input and optical spectral analyzer at the SOA output. Some results are depicted in Fig. 3, where the net gain and the output power of the 750 μm SOA (same as in the third stage of the 8 × 8 OS) are plotted as functions of the input power. These measurements are taken at room temperature, by tuning the laser at 1300 nm wavelength and biasing the SOA at 100 mA. As it is seen from the plots, the SOA opportunely delivers few mW output power at a net gain above 25 dB, still not reaching the saturation.

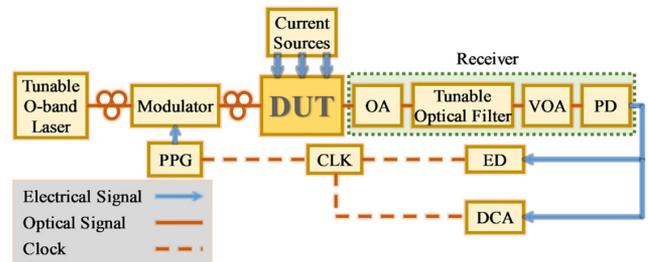
Second, the continuous wave (CW) performance of the packaged OS is explored. In these measurements, a tunable O-band laser operating at 1310 nm wavelength is coupled to the input port of the OS also via the PC and polarization-maintained fiber, which ensured launching a TE optical mode in the input waveguide. The OS output is monitored using an OSA. The set-up insertion loss is measured at 3 dB per facet. The results are summarized in Fig. 4. Figure 4(a) shows the transmitted light



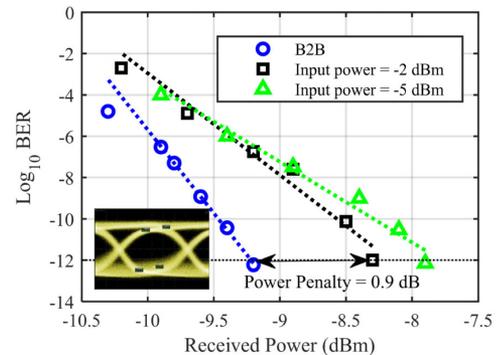
**Fig. 4.** (a) Measured output spectra of the OS, (b) fiber-to-fiber loss as a function of SOA's bias current, (c) OSNR versus SOA's current, (d) normalized output power versus current bias of each stage, (e) fiber-to-fiber loss/gain versus input power.

spectra for the  $I_7$  to  $O_7$  optical path when the input power is set at  $-5$  dBm. This is the optical path with the highest insertion loss, which varies from path to path because of differences in routing. The optical gain at 1310 nm and the ASE noise floor both increase with the SOA bias current. Figure 4(b) presents the fiber-to-fiber loss versus SOA bias current for different values of input power. Lossless operation of the OS is achieved if the SOAs are biased at 70 mA or higher current. Figure 4(c) gives the output OSNR measured with 0.1 nm bandwidth resolution at different input powers. The OSNR increases with the SOA bias, driven by the increase of gain, then saturates and eventually decreases because of a rise of ASE which grows with the bias at a rate greater than that of the gain. Still, even at  $-5$  dBm input power the OSNR exceeds 30 dB. To characterize the extinction ratio (ER) of the switch, the output power is measured from the OFF (zero bias) to ON (70 mA bias) state. The results are plotted in Fig. 4(d), from which it is seen that each stage SOA provides at least  $\sim 24$  dB ER. Employing a control system capable of applying negative voltage bias in the OFF state, the ER may be increased. Finally, Fig. 4(e) presents the fiber-to-fiber net loss as a function of the input optical power while we increase  $I_{SOA3}$  to its maximum value, i.e., 100 mA, to achieve the highest gain. As the input power increases, the net gain provided by the SOAs decreases, in line with the stand-alone SOA characterization. The switch exhibits lossless operation or fiber-to-fiber gain for input powers below  $-4$  dBm. From Fig. 4(e), when the input power to the chip changes from  $-20$  dBm to  $-5$  dBm, the gain variation remains below 5 dB with the optical output power varying from  $-14$  dBm to  $-4$  dBm.

Third, the NRZ PRBS-31 transmission through the packaged  $8 \times 8$  OS is tested. The setup is depicted in Fig. 5. A pulse



**Fig. 5.** Experimental setup for the transmission measurements.



**Fig. 6.** Measured BER as a function of the average received optical power. Inset: output eye diagram recorded at input power =  $-5$  dBm.

pattern generator (PPG) generates a 10 Gbps nonreturn-to-zero (NRZ) PRBS-31 signal. On a transmitter side, a modulated input signal is coupled to the device under test (DUT) in a quasi-TE polarization, maintained by a PC, while current sources bias the SOAs. On the receiver side, an optical amplifier (OA), a tunable O-band optical filter, and a variable optical attenuator (VOA) are inserted between the OS output and the 40 GHz photo detector (PD). The tunable optical filter reduces the broadband ASE noise. The OA and VOA compensate for the insertion loss of the tunable optical filter (around 8 dB) and to control the detected signal, respectively. An internal clock synthesizer (CLK) provides the clock to the PPG and triggers the digital communication analyzer (DCA) for recording eye diagrams and the error detector (ED) for counting bit errors. The measured bit error rate (BER) as a function of the average received optical power for NRZ PRBS-31 transmission from input  $I_7$  to output  $O_7$  is shown in Fig. 6. Similar results are recorded for all other optical paths, demonstrating an error-free data transmission from any input to any output. The power penalty at  $-2$  dBm input power is 0.9 dB. It is mainly due to ASE defined degradation of OSNR and could be further reduced by increasing the input power, but that was beyond the testbed limitations. However, such a reduction of the power penalty would reduce SOA gain, which should be compensated with higher SOA biases to maintain the fiber-to-fiber loss unchanged. For the same reason, the power penalty increases with decreasing of the input power. Still, a clear open eye diagram is recorded at an input power  $-5$  dBm (see Fig. 6 inset), when SOAs are biased at 70 mA each.

The effect of the SOA bias on the NRZ PRBS-31 transmission is also investigated. For this purpose, the transmission test is performed under different SOA bias conditions for two

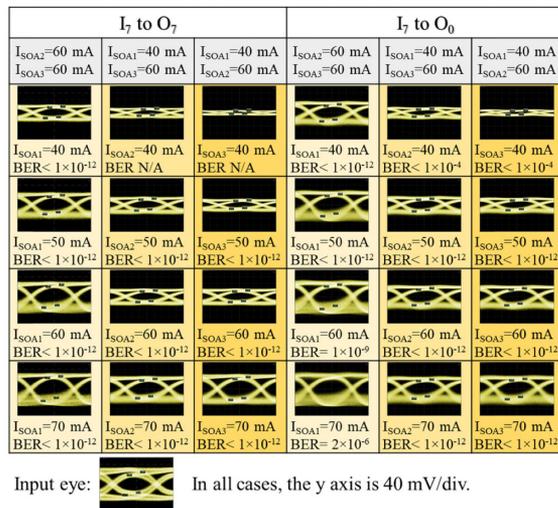


Fig. 7. Eye diagrams for 10 Gbps NRZ PRBS-31 transmission.

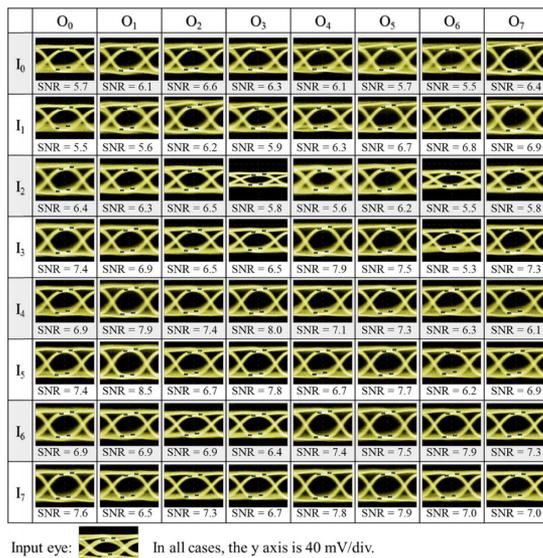


Fig. 8. Eye diagrams for 10 Gbps NRZ PRBS-31 transmission over all 64 optical paths of the  $8 \times 8$  OS.

optical paths:  $I_7$  to  $O_7$  and  $I_7$  to  $O_1$ . In both cases, the input optical power is set at -5 dBm. The results are shown in Fig. 7 demonstrating that for both paths, error-free transmission can be achieved with sufficient bias currents. In the case of the  $I_7$  to  $O_1$  path exhibiting lower shuffling loss between the stages, further increase in the first stage SOA bias can boost the ASE at the input of the second stage, leading to an increase of the zero-level noise and BER. Figure 8 demonstrates the resulting error-free transmission over all 64 optical paths, from any input to any output. The signal-to-noise ratio (SNR) for each recorded eye diagram is calculated by the DCA. In these measurements, the input power is set at -5 dBm, while the SOA biases are adjusted to highest SNR for zero fiber-to-fiber loss. As Fig. 8 reveals, an excellent operation of all 64 optical paths, including 48 SOAs, can be achieved with zero net loss. The lower peak-to-peak in

$I_2$  -  $O_3$  eye diagram is related to a higher shuffling loss in this path, likely due to extra SOA to SE-PWG coupling loss.

Lossless operation of the OS for the most lossy path is achieved when the SOAs are biased at 70 mA or higher current. The voltage of the SOA<sub>1</sub>, SOA<sub>2</sub>, and SOA<sub>3</sub> at 70 mA bias current is 1.7 V, 1.7 V, and 2.2 V, respectively; hence the OS power consumption for lossless operation is at most 392 mW per path for a maximum of 3.14 W for an OS configuration where all paths are active. Unless the PIC sits on temperature-controlled stage, self-heating may lead to degradation of gain and hence further increase of the power consumption required for a lossless operation. The current design is intended for operation with temperature controller.

In summary, a monolithically integrated  $8 \times 8$  OS PIC in InP is designed, fabricated, and characterized. It is based on SOA ON-OFF gate-switching and implemented in a commercial regrowth-free TAVI platform. It is shown that the OS can operate in a truly lossless mode, with zero fiber-to-fiber loss and high (30+ dB per SOA gate) extinction ratio. With wide-open eyes and OSNR greater than 30 dB for all 64 input to output paths in 10 Gbps NRZ PRBS-31 transmission, the OS PIC demonstrates the performance, suggesting potential of the technology for applications in scalable photonic switching.

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