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Modeling the Reverse Gate-Leakage Current in GaN-Channel HFETs: Realistic Assessment of Fowler-Nordheim and Leakage at Mesa Sidewalls

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***Abstract*— A model considering different leakage paths for describing the reverse gate-leakage in mesa-isolated polar GaN-channel heterostructure field-effect transistors (HFET) is presented. For AlGaN/GaN HFETs, it is illustrated that for small negative values of gate-source bias, gate-leakage happens from the gate-covered mesa sidewalls to the 2-D electron gas (2-DEG). The bias- and temperature-dependences of the gate-current show that the sidewall path to the 2-DEG is associated with the Poole-Frenkel electron emission. As the gate-source bias becomes more negative, electrons choose a different path to the 2-DEG. In this case, results corroborate that the gate-leakage is dominated by the Fowler-Nordheim (FN) direct tunneling process through the III-Nitride barrier. The novel contribution of the present analysis is that it postulates that in absence of absolute uniformity, FN tunneling takes place through only a small portion of the surface of the barrier, which boasts the highest electric field or the smallest Schottky barrier height. By applying this hypothesis, the origin of the inconsistencies inherent to the previously presented models in selecting the value of the electron effective mass can be explained.**

***Index Terms*—III-Nitride heterojunction field-effect transistor (HFET), gate-leakage, leakage at mesa sidewalls, Fowler-Nordheim, Poole-Frenkel.**

I. Introduction

UNDRESTANTDING the origin of the excessive reverse gate-current in GaN-channel heterostructure field-effect transistors (HFETs) has been considered to be of enormous importance to the development of these devices [1]. Considering numerous electron transport mechanisms, thus far several models have been developed to explain this device characteristic. When the electric field across the barrier is weak, transport mechanisms which rely on the existence of traps, such as trap-assisted tunneling [2], and Poole-Frenkel (PF) emission [3], [4], are more likely to become dominant. However, the dominance of Fowler-Nordheim (FN) tunneling, as a direct tunneling process, is correlated with the presence of a strong electric field across the barrier [5]. In addition to when a sizable bias is applied between the gate and the source contact, this condition is easily satisfied in polar III-Nitride HFETs enjoying large spontaneous/piezoelectric polarization at the hetero-interface (e.g., in $Al_xGa_{1-x}N$/GaN HFETs with high aluminum mole fraction or ternary lattice-matched $In_{0.17}Al_{0.83}N$/GaN HFETs) [5]-[7]. Thermionic field emission can also challenge the other competitors when electron temperature is sufficiently elevated [1], [2].

In addition to the various transport mechanisms, different leakage paths have also been proven to be worthy of consideration in the evaluation of the gate-leakage of III-Nitride HFETs [8]-[13]. Although conduction through the Al(In)(Ga)N barriers has been widely considered to be the main leakage path, evidence of the existence of a leaking path between the gate-covered mesa-sidewalls and the 2-D electron gas (2-DEG) has been also presented [8].

In the present study, in an attempt to outline a model with realistic set of assumptions for describing the reverse gate-current of GaN-channel HFETs, in addition to the leakage taking place through the III-Nitride barrier, the path via the mesa sidewalls is considered. To assess the validity of the assumptions, and to determine the dominant electron transport mechanism in each identified path, temperature- and bias-dependence of the assumed electron transport processes are analyzed. In case of FN, the previously reported inconsistencies in adopting the constants of the model are also thoroughly discussed [3].

Section II provides the background on the presence of competing paths for gate-leakage in AlGaN/GaN HFETs. Sections III and IV present the discussion on the determination of the dominant electron transport mechanism in each recognized leakage paths. Conclusion is presented in section V.

II. Leakage via the Barrier and Conduction through the Mesa-Sidewalls

As outlined in [8], based on the study of three groups of polar $Al_{0.3}Ga_{0.7}N$/GaN HFETs of different isolation-feature geometry (known as fin, 7-island, and 14-island) built on a common layer structure, the authors have already presented evidence on the existence of a leakage path between the

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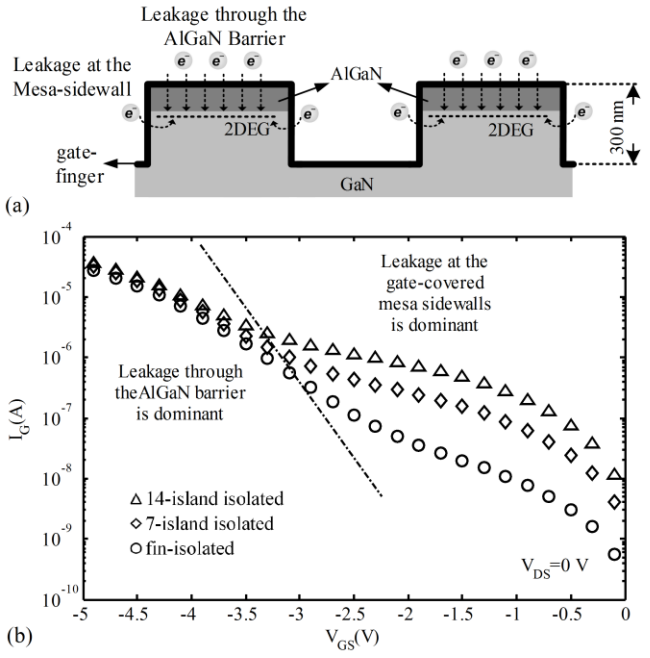

Fig. 1. (a) Gate-dissected cross-sectional view of an island-isolated HFET. The schematic depicts only two of the islands. In case of fin-isolated HFET, the isolation feature is a narrow continues mesa. The two leakage paths discussed in this study are also illustrated. (b) Measured I_G versus V_{GS} for the fin-, 7-island, and 14-island AlGaN/GaN HFET varieties. Measurements were performed at room temperature and drain-source voltage (V_{DS}) of 0 V.

sidewall covering gate-electrode and the 2-DEG. In the present study, using these structures, it has been attempted to model the observed gate-leakage characteristics of AlGaN/GaN HFETs in presence of a number of gate-covered mesa sidewalls. Details of the layer structure and the fabrication process have been reported in [14]. The etched sidewalls of the isolation-features have not been passivated. With the exception of the structure of the isolation-feature, there has been no difference in the fabrication recipe of these transistors. All of the considered device varieties effectively present the same gate-width of about 100 μm and mesa height of 300 nm. Whereas among the fin-isolated devices the isolation-feature is a continuous mesa, in case of the 7-island and the 14-island varieties the total gate-width is divided into 7 and 14 mesas of respectively smaller width. As a result, among these devices the gate electrode covers 2, 14, and 28 sidewalls, respectively. The gate-length among all these devices, unless indicated otherwise, is 0.5 μm. Figure 1(a) illustrates the gate-dissected cross-sectional view of a typical island-isolated HFET. While in the present manuscript these HFETs are employed as test structures for the analysis of gate current, it has been shown that the implementation of GaN-channel HFETs on array of very small size isolation-features, instead of a continuous mesa, is capable of offering enhancement-mode characteristics and a reduced degree of self-heating [15], [16].

Figure 1(b) depicts plots of the room temperature measured gate-current (I_G) for the aforementioned groups of transistors. As mentioned in [8], a correlation between the number of gate-covered sidewalls and I_G is only observed for smaller gate-source biases. For gate-source voltages (V_{GS}) where there is no tangible difference among the reported values of I_G, the common phenomenon of leakage through the equally wide barrier is expected to be responsible for the gate current. Furthermore, as discussed in [8], whereas the HFETs built on similar isolation-feature geometries with different drain and source access regions demonstrate identical I_G, the surface leakage from the gate to the drain and source is not deemed dominant among the explored devices.

Formulating a gate-current model, considering the two aforementioned paths for leakage, requires the identification of the dominant transport mechanism across each path. In the next two sections, relying on the experimental data from the devices mentioned in this section, and a few published sets of data, it is attempted to present a realistic assessment of the dominant transport processes.

III. The Dominant Leakage Mechanism through the Polar III-Nitride Barrier

For large negative values of V_{GS}, due to the presence of strong electric field across the barrier, the Fowler-Nordheim (FN) tunneling process through the barrier has been deemed the most probable contributor to I_G [5]-[8]. While there is consensus on this matter, often in formulating the current density according to this process unrealistic assumptions about certain constants seem inevitable. The FN current density is given by [3], [17]

$$J_{FN} = AE^2 \exp\left(-\frac{8\pi\sqrt{2m_n^* q}}{3hE}\phi_b^{3/2}\right) \quad (1)$$

for $A = \frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$ in which, q is the fundamental electronic charge, h is Planck's constant, m_0 is the free-electron mass, m_n^* is the conduction-band effective mass in the barrier layer, $q\phi_b$ is the Schottky barrier height, and E is the electric field across the barrier. Assuming a triangular approximation for the shape of the polar III-Nitride barrier, electric field E is approximately given by [2],

$$E = \frac{\phi_b - V_{GS} - \Delta\phi_c + \phi_F}{d_{barrier}} \qquad \text{for } V_{GS} > V_{th} \quad (2)$$

in which, $q\Delta\phi_c$ is the conduction-band discontinuity at the barrier/channel hetero-interface, $q\phi_F$ is the difference between fermi energy level and conduction-band edge at the GaN side, $d_{barrier}$ is the barrier thickness, and V_{th} is the threshold-voltage of the HFET. For the fin variety of the AlGaN/GaN HFETs discussed in section II, V_{th} is about -4.5 V [14]. Due to depletion of the 2-DEG at gate-source biases lower than the threshold-voltage, the electric field across the barrier becomes almost independent of V_{GS}. While in here for V_{GS} smaller than V_{th} the electric field is assumed constant, such an assumption limits the accuracy of the model for $V_{GS} << V_{th}$. Although ϕ_F is a function of V_{GS} [18], for values of V_{GS} close to V_{th} (when the higher subbands are not populated) it can be assumed to remain unchanged with bias. Coincidently, as marked in Fig. 1 for the group of polar AlGaN/GaN HFETs, this is the regime

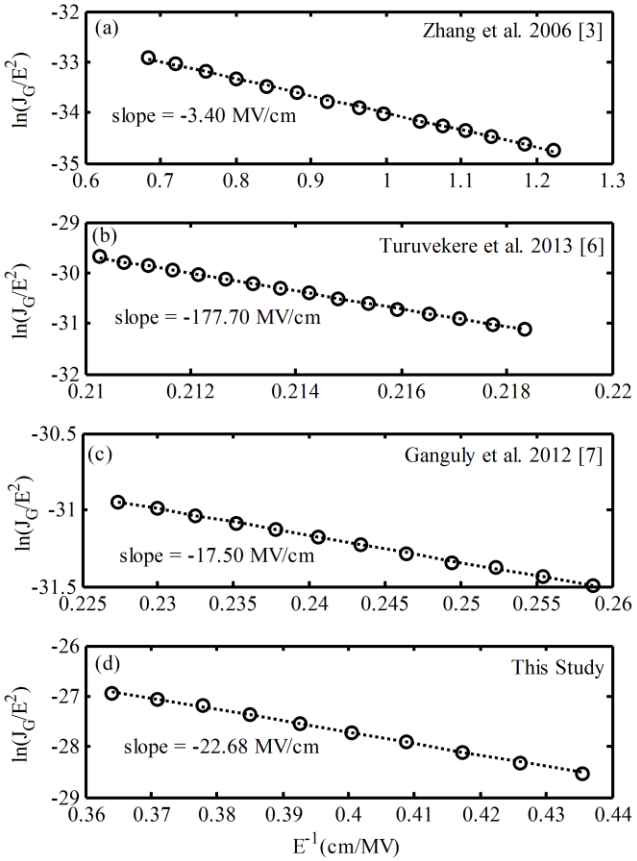

Fig. 2. (a), (b), and (c), show the ln(J_G/E^2) vs. 1/E data collected from [3], [6], [7], respectively. The data from the fin-isolated devices of the present study are given in (d). Symbols represent the experimentally acquired data points and the dotted lines illustrate the linear interpolation among these points.

where leakage through the barrier becomes dominant.

According to (1), the linear dependence of ln(J/E^2) vs. 1/E is counted as an evidence of the dominant presence of FN tunneling [3], [5]-[7], [17]. Therefore, the slope of this linear characteristic is expected to be proportional to $\sqrt{m_n^*}\phi_b^{3/2}$, while its intercept with the vertical axis is defined in terms of $m_n^*\phi_b$. However, for both polar AlGaN/GaN and InAlN/GaN HFETs extraction of the values of m_n^* and ϕ_b through modeling the experimentally recorded FN-dominated gate-current has resulted in evident inconsistencies [3], [6], [7], [19], [20]. In order to assess the cause(s) of this problem, in addition to the data gathered from the fin variety of the devices identified in section II, measurements reported in three representative studies on FN-dominated I_G in AlGaN/GaN and lattice-matched InAlN/GaN HFETs are scrutinized [3], [6], [7]. Figure 2 presents the linear region of ln(J_G/E^2) vs. 1/E for the mentioned studies, where J_G is the gate-current density. Specifications of the barrier layer in each of these studies, along with the extracted (or adopted) values of m_n^* and $q\phi_b$ from Fig. 2 are presented in Table I. The extractions have been carried out based on the slope of the characteristics demonstrated in Fig. 2.

While as indicated in Table I, the values of the adopted parameters into each model are not drastically different from the expected values from literature, the calculated amount of gate leakage, expressed in terms of the ratio of the extracted value of A in (1) to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$, is commonly observed to be many orders of magnitude different from what is experimentally recorded. In addition, it is observed that among the extracted and the expected values of m_n^* and ϕ_b quite often a difference is present. Among these, the worst example is the controversially small value of m_n^* reported in [3].

Among these data, Ganguly *et al.* have argued that the lower than expected extracted value of $q\phi_b = 0.7eV$, in the case of a lattice-matched $In_{0.17}Al_{0.83}N$/GaN HFET [7], is due to microscopic In-composition fluctuations in the InAlN barrier [24], [25]. Accordingly, as long as the expected J_G is greater than the measured value (i.e. unlike [6]), this observation can be attributed to the possibility of a relatively small fraction of the surface of the barrier (associated with high In-composition) being responsible for the FN tunneling.

In each of the cases highlighted in Table I, there exists a similar correlation between the two observed discrepancies (i.e. of the vertical axis intercept and the required value of the effective mass or the Schottky barrier height). A seemingly reasonable explanation for these observations lies in the presence of the exponential term in (1). While J_{FN} dramatically changes with $q\phi_b$ and E, the presence of a degree of non-uniformity across the surface allows the electric field and the Schottky barrier height to be position dependent. Accordingly, the FN tunneling through a part of barrier which

TABLE I
BARRIER STRUCTURE AND THE ADOPTED/EXTRACTED PARAMETERS FOR THE OBSERVED FN LEAKAGE THROUGH THE BARRIER.

Barrier Structure	$q\phi_b$ (eV)	m_n^*/m_0	Ratio of the extracted value of A in (1) to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$	Ref.
$Al_{0.25}Ga_{0.75}N$ 25nm	1.17(a) agreeing with [21] for Ni	0.0016(e) widely different from 0.4 reported in [22]	6.04×10^{-11}	[3]
$In_{0.17}Al_{0.83}N$/AlN 10nm/1nm	2.56(e) larger than 1.46 reported in [23] for Ni	0.4(a) slightly over the accepted range [22]	1.15×10^{9}	[6]
$In_{0.17}Al_{0.83}N$/AlN 7.5nm/1nm	0.7(e) smaller than 1.46 reported in [23] for Ni	0.2(a) within the accepted range [22]	1.74×10^{-7}	[7]
$Al_{0.3}Ga_{0.7}N$/AlN 20nm/1nm	1.23(a) agreeing with [21] for Ni	0.0593(e) widely different from 0.4 reported in [22]	3.80×10^{-4}	This study[1]
$Al_{0.3}Ga_{0.7}N$/AlN 20nm/1nm	1.23(a) agreeing with [21] for Ni	0.4(a) within the accepted range [22]	3.80×10^{-4}	This study[2]

[1]Considering E as estimated by (2).
[2]Considering E as 2.60 times of the value estimated by (2).
Superscripts (a) and (e) stand for adopted and extracted, respectively.

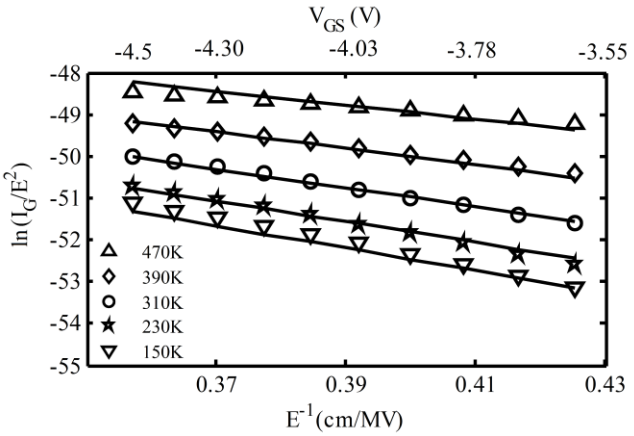

Fig. 3. $\ln(I_G/E^2)$ vs. E^{-1} over wide range of temperature and when FN is dominant. Symbols represent experimental data points. Curves present the calculated values on the assumption of (5). V_{DS} is equal to 0 V.

boasts smaller $q\phi_b$ and/or larger E can dominate the total current density. This portion of the surface of the barrier, corresponding to what has been also reported in case of GaN Schottky diodes [26], can be referred to as *"FN leakage zone"*. Here, it is suggested that the FN leakage zone occupies only a portion of the gated area of the top surface of the barrier, given by the ratio of the extracted A to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$. While the proportion of the total area responsible for FN gate-leakage presents a chance for explaining the smaller than 1 values of the ratio of the extracted value of A in (1) to the calculated value of $\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}$ (presented in Table I), the corresponding number greater than 1 which was reported from [6] remains puzzling. Table I also presents an example on the role of E in assessing the effective electron mass in case of the devices mentioned in section II. According to the data presented on the final row of this table, for both $q\phi_b$ and m_n^* to take realistic values, the electric field needs to be almost 2.6 times as strong as the value calculated by (2). In the remainder of the manuscript, this ratio is expressed by γ. In this case, if the *FN leakage zone* of stronger electric field takes on only 0.038 percent of the gated surface area, not only the discrepancy on the effective mass but also on the readout of the y-intercept will be eliminated.

In an attempt to substantiate the proposal on the existence of a FN leakage zone, the gate-currents among two groups of devices with the gate length of 0.5 and 1 μm have been compared. Both groups shared the same value of gate width, as indicated in section II. Both groups of HFETs presented almost the same amount of gate-leakage (i.e. independent of 100 percent increase in the area of the gate electrode). This observation corroborates the proposed hypothesis of the existence of a FN leakage zone, according to which the whole gate area is not considered to be involved in the FN process. Since the area of the proposed FN leakage zone does not change considerably with the 100 percent increase of the total gate area, in correlation with a negligible increase in the perimeter of this gate covered area, the expected region of higher E can be attributed to this periphery. Barrier thinning due to the presence of surface defects can be one of the reasons for the generation of FN leakage zone [27].

TABLE II
PARAMETERS USED IN EXPRESSING THE FOWLER NORDHEIM TUNNELING CURRENT THROUGH THE BARRIER OF ALUMINUM COMPOSITION OF 0.3 ACCORDING TO (4) AND (5).

Sym.	*Definition*	*Value*	Ref.
ϕ_b at T=300 K, E=0 V/m	Ni/barrier Schottky barrier height	1.23 eV	[21]
m_n^*	Conduction-band effective mass in $Al_{0.3}Ga_{0.7}N$	0.4 $\times 9.11\times10^{-31}$ kg	[22]
α	Varshni empirical constant	1.4 meV/K	[30], [31]
β	Constant defined in association with the Debye temperature	860 K	[30], [31]
ε_r	relative dielectric constant	10.31	[21]
γ	Magnification of E across the FN leakage zone	1.8039	Extracted
S_{FN}	FN leaking zone area	6.02×10^{-14} m^2	Extracted

While the hypothesis on the existence of a FN leakage zone provides reasonable evidence on the dominance of FN process (i.e. when a large negative V_{GS} is applied) without any need for invoking unreasonable assumptions, the dominance of FN is still needed to be substantiated via studying the temperature dependence of the I_G. In spite of the temperature independence of quantum tunneling, the temperature dependence of the concentration of impinging charge carriers is still responsible for making the FN process a function of temperature [17]. This effect is modeled by incorporating a multiplicative term of $\pi ckT/\sin(\pi ckT)$ in (1), in which k is the Boltzmann constant, T is the temperature in Kelvin and c is defined as:

$$c = \frac{4\pi\sqrt{2m_n^*\phi_b}}{hE}. \quad (3)$$

The existence of E in the definition of c has a negligible impact on the linear characteristics reported in Fig. 2. Considering the effect of temperature on $q\phi_b$ and the barrier-lowering due to presence of image forces at the metal-barrier contact, $q\phi_b$ can be represented by [28], [29]

$$q\phi_b = q\phi_{b0} - \frac{\alpha T^2}{\beta+T} - \sqrt{\frac{q^3E}{4\pi\varepsilon_r\varepsilon_0}} \quad (4)$$

in which, α is the Varshni empirical constant, β is a constant defined in close association with the Debye temperature, and ϕ_{b0} is selected in a way that at T = 300K and zero E, $q\phi_b$ reaches the typical value mentioned in [21] as a function of the Al composition. ε_0 is the permittivity of vacuum, and ε_r is the relative permittivity of the barrier. Applying these factors, in order to explain the temperature dependence of the FN process, (1) is modified to,

$$I_{FN} = S_{FN}\frac{q^2(m_0/m_n^*)}{8\pi h\phi_b}\frac{\pi ckT}{\sin(\pi ckT)}(\gamma E)^2 \times \exp\left(-\frac{8\pi\sqrt{2m_n^*q}}{3h\gamma E}\phi_b^{3/2}\right) \quad (5)$$

where S_{FN} stands for the area of the FN leakage zone.

Figure 3 presents $\ln(I_G/E^2)$ vs. $1/E$ for the AlGaN/GaN HFETs identified in section II over a wide range of temperature. The room-temperature value of the parameters taken into account for presenting the data points of Fig. 3 in term of (5) are summarized in Table II. As shown in Fig. 3, these same values have been proven to be well suited to express the value of I_G at other temperatures from 150 to 470 K.

IV. Dominant Leakage Mechanism at Gate-Covered Mesa Sidewalls

Whereas the FN based model presented in the previous section seems capable of accurately forecasting the amount of gate-leakage for more negative values of V_{GS}, as highlighted in Fig. 1 for values of V_{GS} closer to 0 V existence of a certain correlation with the number of gate-covered sidewalls rules out the dominance of FN across the barrier [8]. For this latter range of V_{GS}, the study of temperature dependence of Pool-Frenkel (PF) electron emission taking place between the gate-covering mesa sidewall and the 2-DEG, among the AlGaN/GaN HFETs mentioned in section II seems to provide sufficient evidence on the dominance of this mechanism. It must be highlighted that due to the presence of Fermi-level pinning at the non-polar III-Nitride surfaces [32], and also barrier thinning at these sidewalls (caused by the inevitable deviation from vertical etching of the sidewall), at these positions the gate electrode cannot be in direct contact with the 2-DEG.

In order to formulate the PF process at the mesa sidewall, the electron emission is in here assumed to take place from a trap state close to the gate metal at the mesa-sidewall into a continuum of states in GaN. It is then through this continuum of states that electrons reach the 2-DEG [9], [33]. The damage caused by inductively-coupled plasma etching (ICP), which is used to form the isolation-features, contributes to the formation of the aforementioned traps close to the sidewalls. The PF current density is presented by [3], [33],

$$J_{PF} = C_{PF} E_{sidewall} exp\left(-\frac{q(\phi_t - \sqrt{qE_{sidewall}/\pi\varepsilon_0\varepsilon_s})}{kT}\right) \quad (6)$$

in which, in addition to the aforementioned parameters, ε_s is the relative high frequency permittivity of GaN, $q\phi_t$ is the barrier height for electron emission from the trap state, and C_{PF} is a constant.

In (6), $E_{sidewall}$ is the electric field defined in terms of the potential difference between gate and the 2-DEG. This electric field depends on several parameters including the slope of the sidewall and the strain relaxation in the vicinity of the mesa edge. The maximum $E_{sidewall}$ is defined where the gate metal covering the mesa sidewall and 2-DEG are at the minimum distance. Considering the exponential dependence of PF on the electric field, $E_{sidewall}$ is estimated as a one-dimensional electric field defined at the depth of the 2-DEG channel. However, when considering the Fermi-level pinning at the less than vertically defined sidewalls, assuming the linear definition of this one-dimensional electric field in terms of V_{GS} poses considerable challenge on accurate evaluation of the length of the region across which this bias is applied. In the present study, assuming vertical sidewalls and negligible dopant concentration in the channel, the following first order assumption is used for calculation of $E_{sidewall}$,

$$E_{sidewall} = m_{PF} V_{GS} \quad \text{for } V_{GS} > V_{th} \quad (7)$$

in which, m_{PF} is the proportionality factor that is used as the only fitting parameter. This equation is deemed approximately valid for the gate-source biases larger than the threshold-voltage. In the absence of a strong 2DEG when $V_{GS} < V_{th}$, the leakage path discussed in this section is no longer dominant.

According to (6), in the presence of PF emission, $\ln(J_{PF}/E_{sidewall})$ is a linear function of $\sqrt{E_{sidewall}}$, where the slope and the vertical axis intercept are functions of T, respectively presented as,

$$a(T) = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_s}} \quad (8)$$

$$b(T) = -\frac{q\phi_t}{kT} + ln\ C_{PF}. \quad (9)$$

When (6) is applicable, according to (8) the plot of a(T) vs. 1/T should present a straight line with a slope capable of providing the value of ε_s, which is projected to 0 at very high

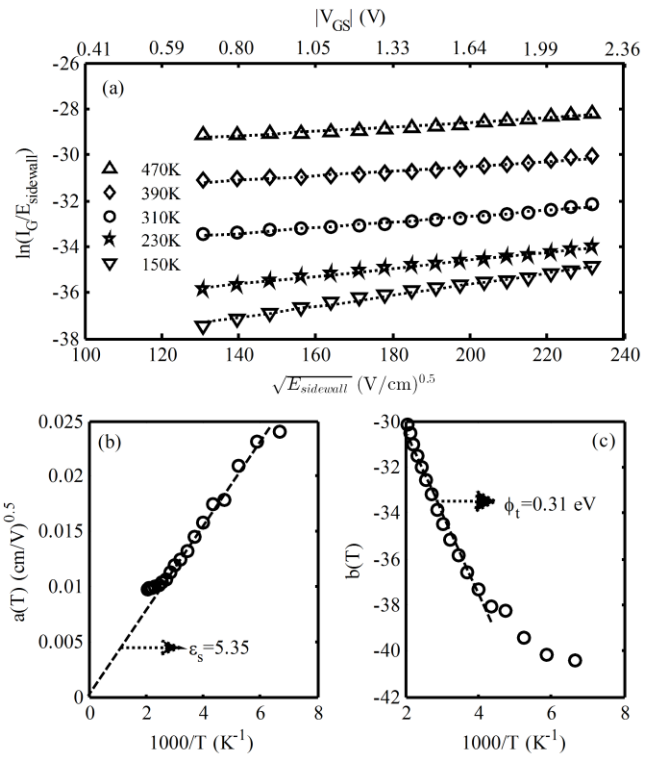

Fig. 4. (a) $\ln(I_G/E_{sidewall})$ vs. $\sqrt{E_{sidewall}}$ over the gate-source regime of bias that the leakage at gate-covered mesa sidewall is dominant. Symbols represent experimental data points. Dash lines are the fitted lines for the presented symbols. (b) and (c) present the slope and y-intercepts of dash lines in (a) vs. 1/T. Only five, out of many temperatures, are presented in (a). V_{DS}=0 V.

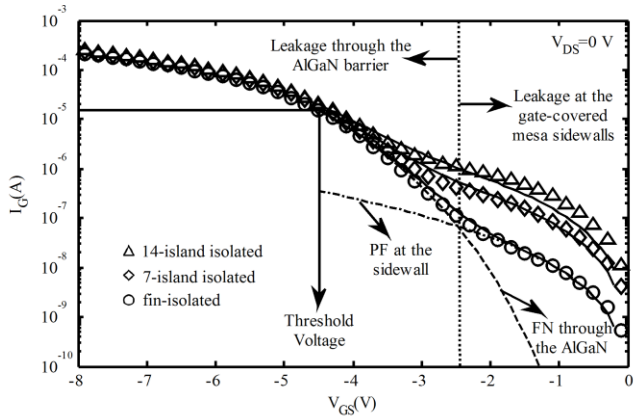

Fig. 5. I_G vs. V_{GS} over the wide range of V_{GS} for the fin-, 7-island, and 14-island AlGaN/GaN HFET varieties mentioned in section II. Symbols represent experimental data points. Dash line is the calculated FN component through the AlGaN barrier (I_{FN}) discussed in section III. Dash-dot line is the calculated PF at the gate-covered mesa sidewalls (I_{PF}) discussed in section IV for the fin-isolated device. Three solid lines are $I_{FN}+I_{PF}$, $I_{FN}+7\times I_{PF}$, and $I_{FN}+14\times I_{PF}$, which present the total gate leakage calculated for the fin-, 7-island, and 14-island device varieties, respectively. V_{DS} is equal to 0 V and gate-length is 0.5 μm.

temperatures. In addition, the slope of b(t) vs. 1/T should be capable of forecasting $q\phi_t$. Although several studies have claimed the observation of PF emission in GaN-channel HFETs, only a few of them have presented the temperature dependence of these factors [3], [7].

For the experimental data from the fin-variety of the devices indicated in section II, Fig. 4(a) shows the linear dependence of $\ln(I_G/E_{sidewall})$ vs. $\sqrt{E_{sidewall}}$, while Figs. 4(b) and (c) depict the variation of a(T) and b(T) with temperature. On these graphs, since the leakage area corresponding to the gate-leakage at gate-covered mesa sidewalls cannot be exactly defined, I_G has been studied instead of J_G. This will only affect the proportionality constant C_{PF}. While the data presented in Fig. 4 across a wide range of temperature satisfies the aforementioned expectations of when the PF process is dominant, the accordingly projected values of ε_s and $q\phi_t$ are respectively equal to 5.35 and 0.31 eV. These values are quite acceptable [3]. As mentioned earlier, m_{PF} is the only fitting parameter employed for the superbly matched model presented in Fig. 5 in terms of the dash lines. In here, the value for m_{PF} has been taken as 2.44×10^6 m^{-1}.

It is worth re-emphasizing that the slope of mesa sidewall can affect the sidewall leakage in different ways. The damage introduced on the mesa sidewalls by the ICP etching, and the contributed trap profile, can be functions of the steepness of the sidewalls. It is also expected that in HFETs of steeper sidewalls, in absence of reduction in polarization-induced 2DEG concentration in the periphery of the tapered sidewalls, larger $E_{sidewall}$ develops as the physical distance between the 2DEG and the gate metal at the mesa sidewall becomes smaller. Reduction in the steepness of mesa sidewall is also expected to affect the degree of strain relaxation in the vicinity of mesa sidewall. As a result, in addition to scaling of the PF-contributed sidewall leakage with device dimensions such as gate length, process-dependent parameters such as sidewall slope are deemed capable of modifying the amount of sidewall leakage from transistor to transistor.

Further to these studies, the authors have also attempted to explain the leakage at the mesa-sidewall using other electron transport mechanisms such as field emission, thermionic field emission, Ohmic conduction, and trap assisted tunneling. However, none of these mechanisms were successful in terms of predicting the observed trends. The relatively smooth voltage dependence of I_G under the dominance of leakage at the mesa-sidewalls contradicts the plausibility of field emission. Similar observation at low temperature (i.e. 150K) discards the chance of thermionic field emission at room temperature. Whereas in this case the plausibility of Ohmic conduction has been also investigated, the non-liner behavior of I-V rejects this possibility.

V. Conclusion

Applying the model described in the previous two sections, the calculated I_G over a wide range of values for V_{GS}, for the fin, 7-island, and 14-island variety of AlGaN/GaN HFETs presented in section II of the manuscript, is provided in Fig. 5. In this figure, the PF leakage component at the isolation-feature sidewall is calculated for the fin-isolated HFET. The PF component for the 7-island, and 14-island HFETs are considered to be 7 and 14 times larger, respectively. Superb matching between the model and the experimental data (highlighting the turning point between the two dominant processes) suggest the accuracy of the presented model. According to this model, while for small negative values of V_{GS}, I_G is dominated by PF electron emission taking place between the gate-covered mesa sidewalls and the 2-DEG, as the gate-source bias gets more negative FN through the AlGaN barrier becomes dominant. Evidence shows that the FN component occurs only in a small portion of barrier (here referred to as FN leakage zone).

References

[1] E. J. Miller, X. Z. Dang, and E. T. Yu, "Gate-leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," *J. Appl. Phys.*, vol. 88, no. 10, pp. 5951–5953, Nov. 2000, doi: 10.1063/1.1319972.

[2] S. Karmalkar, D. M. Sathaiya, and M. S. Shur, "Mechanism of the reverse gate-leakage in AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 82, no. 22, pp. 3976–3978, Jun. 2003, doi: 10.1063/1.1579852.

[3] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, no. 2, pp. 023703-1–023703-6, Jan. 2006, doi: 10.1063/1.2159547.

[4] O. Mitrofanov and M. Manfra, "Poole–Frenkel electron emission from the traps in AlGaN/GaN transistors," *J. Appl. Phys.*, vol. 95, no. 11, pp. 6414–6419, Jun. 2004, doi: 10.1063/1.1719264.

[5] S. Turuvekere, D. S. Rawal, A. DasGupta, and N. DasGupta, "Evidence of Fowler–Nordheim tunneling in gate-leakage current of AlGaN/GaN HEMTs at room temperature," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4291–4294, Dec. 2014, doi: 10.1109/TED.2014.2361436

[6] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. DasGupta, and N. DasGupta, "Gate-leakage mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and modeling," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3157–3165, Oct. 2013, doi: 10.1109/TED.2013.2272700.

[7] S. Ganguly, A. Konar, Z. Hu, H. Xing, and D. Jena, "Polarization effects on gate-leakage in InAlN/AlN/GaN high-electron-mobility transistors,"

Appl. Phys. Lett., vol. 101, no. 25, pp. 253519-1–253519-5, Dec. 2012, doi: 10.1063/1.4773244.

[8] H. R. Mojaver and P. Valizadeh, "Reverse gate-current of AlGaN/GaN HFETs: Evidence of leakage at mesa sidewalls," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1444–1449, Apr. 2016, doi: 10.1109/TED.2016.2529301.

[9] C. Xu, J. Wang, H. Chen, F. Xu, Z. Dong, Y. Hao, and C. P. Wen, "The leakage current of the Schottky contact on the mesa edge of AlGaN/GaN heterostructure," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 942–944, Nov. 2007, doi: 10.1109/LED.2007.906932.

[10] Y.-S. Lin, Y.-W. Lain, and S. S. H. Hsu, "AlGaN/GaN HEMTs with low leakage current and high on/off current ratio," *IEEE Electron Device Lett.*, vol. 31, no. 2, pp. 102–104, Feb. 2010, doi: 10.1109/LED.2009.2036576.

[11] J. Kováˇc, A. Šatka, A. Chvála, D. Donoval, P. Kordoš, and S. Delage, "Gate-leakage current in GaN-based mesa- and planar-type heterostructure field-effect transistors," *Microelectron. Rel.*, vol. 52, no. 7, pp. 1323–1327, Feb. 2012, doi: 10.1016/j.microrel.2012.02.003.

[12] P. Liu, C. Xie, F. Zhang, J. Chen, and D. Chen, "Elimination of gate-leakage in GaN FETs by placing oxide spacers on the mesa sidewalls," *IEEE Electron Device Lett.*, vol. 34, no. 10, pp. 1232–1234, Oct. 2013, doi: 10.1109/LED.2013.2278013.

[13] J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, "Mechanism of surface conduction in the vicinity of Schottky gates on AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 91, no. 9, pp. 093501-1–093501-3, Aug. 2007, doi: 10.1063/1.2775834.

[14] A. Loghmany and P. Valizadeh, "Alternative isolation-feature geometries and polarization-engineering of polar AlGaN/GaN HFETs," *Solid-State Electron.*, vol. 103, pp. 162–166, Jan. 2014, doi: 10.1016/j.sse.2014.08.001.

[15] K. Ohi and T. Hashizume, "Drain current stability and controllability of threshold voltage and subthreshold current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Japanese J. Appl. Phys*., vol. 48, no. 8, pp. 081002-1–081002-5, Aug. 2009, doi: 10.1143/JJAP.48.081002.

[16] A. Loghmany, P. Valizadeh, and J. Record, "Impact of Isolation-Feature Geometry on Self-Heating of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 9 pp. 3152-3158, Sep. 2014, doi: 10.1109/TED.2014.2339011.

[17] M. Lenzlinger and E. H. Snow, "Fowler–Nordheim tunneling into thermally grown SiO_2," *J. Appl. Phys.*, vol. 40, no. 1, pp. 278–283, Jan. 1969, doi: 10.1063/1.1657043.

[18] F. Manouchehri, P. Valizadeh, and M. Z. Kabir, "Determination of subband energies and 2DEG characteristics of $Al_xGa_{1-x}N$/GaN heterojunctions using variational method," *J. Vac. Sci. Technol. A*, vol. 32, no. 2, pp. 021104-1-8, Mar. 2014, doi: 10.1116/1.4865562.

[19] L. Xia, A. Hanson, T. Boles, and D. Jin, "On reverse gate leakage current of GaN high electron mobility transistors on silicon substrate," *Appl. Phys. Lett.*, vol. 102, no.11, pp. 113510-1–113510-4, Mar. 2013, doi: 10.1063/1.4798257.

[20] A. Fontsere, A. Pérez-Tomás, M. Placidi, J. Llobet, N. Baron, S. Chenot, Y. Cordier, J. C. Moreno, M. R. Jennings, P. M. Gammon, C. A. Fisher, V. Iglesias, M. Porti, A. Bayerl, M. Lanza, and M. Nafria, "Nanoscale investigation of AlGaN/GaN-on-Si high electron mobility transistors," *Nanotechnology*, vol. 23, no.19, pp.395204-1–395204-8, Sep. 2012, doi: 10.1088/0957-4484/23/39/395204.

[21] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzman, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 11, pp. 3222–3233, Mar. 1999, doi: 10.1063/1.369664.

[22] Y.-N. Xu and W. Y. Ching, "Electronic, optical, and structural properties of some wurtzite crystals," *Phys. Rev. B*, vol. 48, no. 7, pp. 4335–4351, Aug. 1993, doi: 10.1103/PhysRevB.48.4335.

[23] D. Donoval, A. Chvála, R. Šramatý, J. Kováè, J.-F. Carlin, N. Grandjean, G. Pozzovivo, J. Kuzmík, D. Pogany, G. Strasser, and P. Kordoš, "Current transport and barrier height evaluation in Ni/InAlN/GaN Schottky diodes," *Appl. Phys. Lett.*, vol. 96, no. 22, pp. 223501-1–223501-3, May 2010, doi: 10.1063/1.3442486.

[24] T. D. Veal, C. F. McConville, and W. J. Schaff, Indium Nitride and Related Alloys. New York, NY, USA: CRC Press, 2010, p. 111.

[25] A. Koukitu and H. Seki, "Unstable region of solid composition in ternary nitride alloys grown by metalorganic vapor phase epitaxy," *Japanese J. Appl. Phys.*, vol. 35, no. 12B, pp. L1638–L1640, Dec. 1996.

[26] T. Sawada, Y. Ito, K. Imai, K. Suzuki, H. Tomozawa, and S. Sakai, "Electrical properties of metal/GaN and SiO_2/GaN interfaces and effects of thermal annealing," *Appl. Surf. Sci.*, vol. 159/160, no. 1/2, pp. 449–455, Jun. 2000, doi: 10.1016/S0169-4332(00)00060-X.

[27] T. Hashizume, J. Kotani, and H. Hasegawa, "Leakage mechanism in GaN and AlGaN Schottky interfaces," *Appl. Phys. Lett.*, vol. 84, no. 24, pp. 4884–4886, Jun. 2004, doi: 10.1063/1.1762980.

[28] Y. P. Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*, vol. 34, no. 1, pp. 149–154, 1967, doi: 10.1016/0031-8914(67)90062-6.

[29] R. S. Muller, T. I. Kamins, and M. Chan, Device Electronics for Integrated Circuits. New York, NY, USA: Wiley, 2003, p. 151.

[30] N. Nepal, J. Li, M. L. Nakarmi, J. Y. Lin, and H. X. Jiang, "Temperature and compositional dependence of the energy band gap of AlGaN alloys," *Appl. Phys. Lett.*, vol. 87, no. 24, pp. 242104-1-242104-3, Dec. 2005, doi: 10.1063/1.2142333.

[31] K. B. Nam, J. Li, J. Y. Lin, and H. X. Jiang, "Optical properties of AlN and GaN in elevated temperatures," *Appl. Phys. Lett.*, vol. 85, no. 16, pp. 3489-3491, Oct. 2004, doi: 10.1063/1.1806545.

[32] L. Lymperakis, P. Weidlich, H. Eisele, M. Schnedler, J. Nys, B. Grandidier, D. Stiévenard, R. Dunin-Borkowski, J. Neugebauer, and P. Ebert, "Hidden surface states at non-polar GaN $(10\bar{1}0)$ facets: Intrinsic pinning of nanowires," *Appl. Phys. Lett.*, vol. 103, no.15, pp. 152101-1–152101-4, Oct. 2013, doi: 10.1063/1.4823723.

[33] J. Frenkel, "On pre-breakdown phenomena in insulators and electronic semi-conductors," *Phys. Rev.*, vol. 54, p. 647, Oct. 1938, doi: 10.1103/PhysRev.54.647.