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Drain-bias dependent study of reverse gate-leakage current in AlGaN/GaN HFETs

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***Abstract*—Reverse gate-leakage of the AlGaN/GaN heterostructure field-effect transistors (HFETs) is studied at different values of drain to source voltage (V_{DS}), ranging from 0 to 10 V. Throughout the investigated range of V_{DS}, the reported analysis confirms the applicability of the Fowler-Nordheim (FN) tunneling as the dominant contributor to the gate-leakage for reverse gate biases until the onset of the threshold voltage. Device simulations were performed using Comsol Multiphysics to estimate the electric field (E) across the polar III-nitride barrier layer at different positions along the gate length. We observe that FN tunneling takes place predominantly corresponding to the average electric field observed to be close to E at the center of the gate for lower values of V_{DS}, whereas at larger values of V_{DS}, FN tunneling corresponding to E only at the drain edge of the gate seems poised to deliver the gate-leakage current. In formulating the FN tunneling, the value of the electron effective mass is selected consistently within an acceptable range for analyzing gate-leakage. Investigating the applicability of FN tunneling in explaining the reverse gate-leakage current of AlGaN/GaN HFETs for the aforementioned values of gate to source voltage (V_{GS}) not just at zero V_{DS}, but across a range of V_{DS} values, seems to offer a more convincing argument for the hypothesis on tunneling through small leakage zones.**

***Index Terms*—AlGaN/GaN heterostructure field-effect transistor (HFET), gate-leakage, Fowler-Nordheim (FN) tunneling, FN leakage zone.**

I. Introduction

THE GaN-channel heterostructure field effective transistors (HFETs) have been extensively studied over the past two decades. This interest has been due to the excellent properties of the III-nitride material system, such as high electron saturation velocity, large critical electric field, and large polar 2-D electron gas (2-DEG) concentration [1]. These exemplary material properties make GaN-based devices perfect choices for power electronic and microwave telecommunication applications [2]. However, there are still problems such as excessive gate-leakage that are preventing the full-scale commercialization of this technology [3-8]. Identifying the mechanism(s) responsible for the excessive gate-leakage in AlGaN/GaN HFETs is rightly expected to allow devising design strategies to alleviate this problem.

Whereas depending on bias and temperature various mechanisms other than thermionic- and field-emission (such as Poole-Frenkel emission [3] [5], and trap assisted tunneling [6], which rely on multistep tunneling across the AlGaN barrier) have been reported to contribute to gate-leakage, a direct tunneling mechanism such as Fowler-Nordheim [9-13] has been observed to be dominant when the electric field across the barrier layer is sufficiently strong. The primary goal of the present study is to evaluate at finite values of drain-source bias (V_{DS}) the required assumptions in modeling the gate-leakage when Fowler-Nordheim is convincingly poised to act as the dominant leakage mechanism. The possibility of tunneling aggravates at an elevated drain-source bias. While previous reports have studied this mechanism responsible for gate-leakage in AlGaN/GaN HFETs at zero drain bias [9-13], according to the best of the authors' knowledge, the present study is a first attempt in analyzing FN leakage at drain biases other than zero ranging from 0 to 10 V. To avoid any complication arising from impact ionization processes visible at higher values of V_{DS}, this choice of bias range has been made in an effort to study the transistors when the heterostructure is maintained close to its pristine form [14]. Although, in modeling the leakage it is often observed that an agreeable matching to the experimental data can be produced by selecting unrealistic values of some key parameters (such as electron effective mass or barrier height) at a singular value of drain bias [3], [9], [11], in our approach, we only count a mechanism applicable or dominant when all of the critical parameters are consistently selected with a realistic set of assumptions for analyzing gate-leakage at different values of drain bias. In our view, considering the role of drain bias in inducing nonuniformity to the electric field distribution profile along the channel, this added dimension to the scrutiny in selecting the parameters gives the conclusion of the analysis a stronger assurance.

Whereas application of large drain biases, and consequent development of stronger electric field across the barrier especially at the drain edge of the gate, have been indicated as causes for reliability concerns and constitution of stronger surface component of gate leakage in AlGaN/GaN HFETs [15-

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17], for the applied moderate values of drain bias no such evidence has surfaced.

Since the FN tunneling is quite substantially associated with a large electric field across the barrier layer, it is necessary to accurately estimate the perpendicular to the channel electric field across the barrier layer [8-13], [18]. Device simulations using Comsol Multiphysics [19] were performed to accurately calculate this electric field component at different drain biases. Subsequent to this evaluation, gate-leakage is analyzed by applying the hypothesis reported in our prior work [11], wherein through temperature-dependent study of gate-leakage among GaN-channel HFETs FN tunneling was demonstrated through a small portion of the surface of the barrier, which is promoting higher electric field or smaller Schottky barrier height due to the presence of non- uniformity across the surface. This portion of the surface of the barrier can be referred to as "FN leakage zone" [11], [20]. A possible contributor to the formation of such zones in III-nitride HFETs grown on non-native substrates is the screw dislocations extending up to the channel from the interface between the substrate and the buffer layer. In the different but relevant context of microwave performance, the presence of such dislocations when a buffer layer is present below the channel layer has been reported to have a detrimental impact [21].

Device and measurement details are briefly presented in section II. Section III provides the analysis for determining the contribution of FN tunneling to gate-leakage at all of the considered drain biases. The conclusion is provided in section IV.

II. Device Fabrication and Measurements

The studied devices were fabricated on a Ga-face Wurtzite $Al_{0.25}Ga_{0.75}N$/GaN heterostructure composed of 25 nm thick barrier and 1.7 μm thick GaN buffer (which was Fe doped away from the channel) grown on a 4-inch 4-H-SiC substrate. The major steps of fabrication include: mesa etching, metallization and rapid thermal annealing (RTA) of ohmic contacts, deposition of Schottky gate, and the contact pad deposition. Electron beam lithography of beam energy 20 keV was employed for defining the mesa, as well as ohmic contacts and the gate electrode. Optical lithography was used for defining the contact pads. Mesa isolation of active layers to 300 nm depth was performed employing magnetically enhanced reactive ion etching (MERIE) using Cl_2/Ar plasma. The ohmic metal stack of Ti/Al/Ti/Au of respective thicknesses 250Å/1500Å/400Å/250Å was deposited using electron beam evaporation, followed by liftoff in acetone using ultrasonic bath and rapid thermal annealing for 30 seconds at 850˚C in nitrogen ambient. Following ohmic annealing, Schottky gate stack of Ni/Au (of thicknesses 200Å/200Å) was deposited in the electron beam evaporator and then patterned using the same liftoff process into gate fingers of 0.5 μm length and width equal to 40 μm. Unless otherwise indicated, gate-source spacing (L_{GS}) is 4 μm and gate-drain spacing (L_{GD}) is 6 μm. No surface or sidewall passivation was performed on any of the fabricated devices.

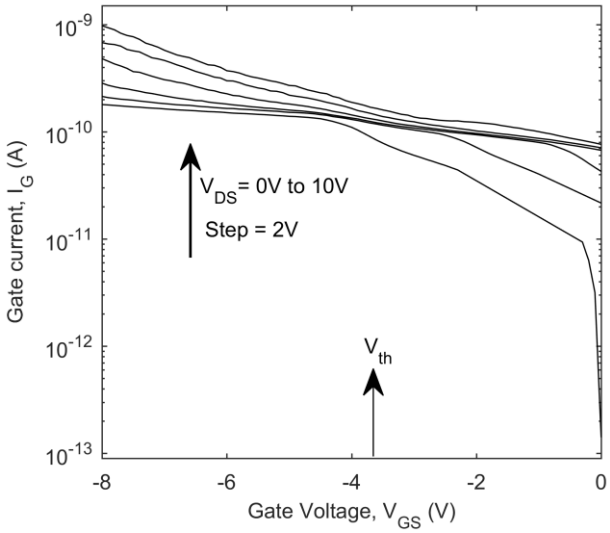

Fig. 1. Experimental I_G versus V_{GS} at different values of V_{DS}. Measurements were performed at room temperature.

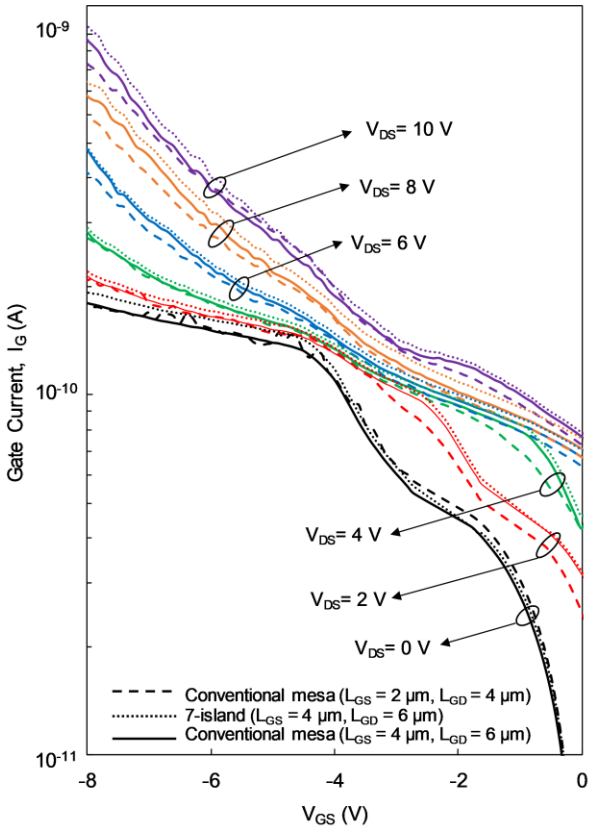

Fig. 2. Experimental I_G versus V_{GS} for 7-island isolated and mesa isolated devices with different length of access regions at different values of V_{DS}.

Keithley 4200-SCS semiconductor characterization system was used for on-chip characterization of a large number of identical AlGaN/GaN HFETs at room temperature. Figure 1 shows a representative set of measured gate current-voltage characteristics at different drain biases. In order to substantiate whether or not leakage paths other than the one envisioned through the AlGaN barrier (for example those defined in association with the isolation mesa geometry and surface

TABLE I
MATERIAL PROPERTIES USED IN SIMULATIONS

Parameter	Value ($Al_{0.25}Ga_{0.75}N$ barrier layer)	Value (GaN layer)	Value (Ni/Au Schottky gate contact)	Reference
Static relative permittivity (ε_r)	8.8	8.9	-	[1],[22]
Bandgap (E_g)	3.9 (eV)	3.39 (eV)	-	[1],[25]
Electron affinity (χ_0)	3.2 (eV)	4.1 (eV)	-	[1],[25]
Effective density of states, Valance band (N_{V0})	4.6×10^{19} (cm^{-3})	4.6×10^{19} (cm^{-3})	-	[1],[25]
Effective density of states, Conduction band (N_{C0})	2.3×10^{18} (cm^{-3})	2.3×10^{18} (cm^{-3})	-	[1],[25]
Electron mobility (μ_n)	600 ($cm^2V^{-1}S^{-1}$)	1000 ($cm^2V^{-1}S^{-1}$)	-	[1],[25]
Hole mobility (μ_p)	40 ($cm^2V^{-1}S^{-1}$)	200 ($cm^2V^{-1}S^{-1}$)	-	[1],[25]
Work function (ϕ_m)	-	-	5.2 (eV)	[26]
Schottky barrier height (ϕ_B)	-	-	1.07 (eV)	[26],[27]

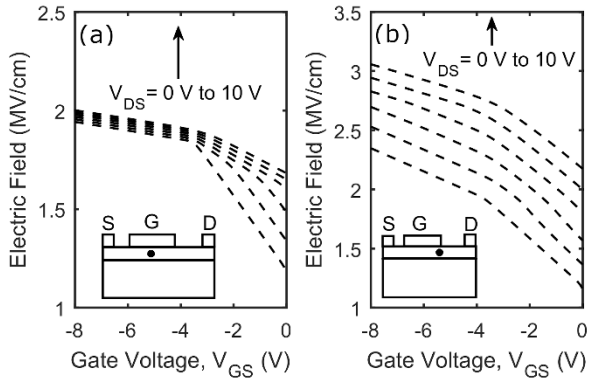

Fig. 3. Simulated vertical Electric field read halfway through the barrier thickness underneath the gate electrode as a function of V_{GS} at different values of V_{DS}. (a) Readout at the center of the gate (see inset). (b) Readout from the drain edge of the gate (see inset).

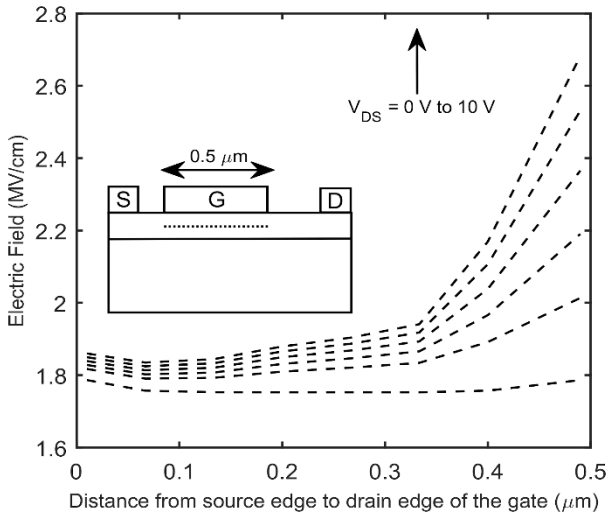

Fig. 4. Simulated electric field distribution at different values of V_{DS} along a horizontal cut running through the middle of the AlGaN barrier (see inset). V_{GS} is equal to -3 V and gate-length is 0.5 μm.

leakage) are playing a tangible part in establishing the gate leakage, not only transistors built on a continuous conventional mesa but also those that for the same total gate width are built on an array of seven individual small islands are studied. According to the consistently observed data presented in Fig. 2, over a wide range of gate to source voltage (V_{GS}) and V_{DS}, for V_{GS} values well below the threshold voltage (where FN tunneling is often observed to be dominant) almost similar gate-leakage current is observed among HFETs fabricated on conventional continuous mesas (of different lengths of the source and drain access regions) and those fabricated on the array of 7 small islands. While in devices built on an array of small mesas the gate electrode is exposed to many more unpassivated side walls, these observations prove the existence of no substantial influence of mesa geometry. Considering the absence of substantial influence from the variation of the length of the access regions, the same can be said about the contribution of the surface leakage.

The threshold voltages of the devices are consistently observed to be about -3.6 V, while the normalized maximum extrinsic gate transconductance is 140 mS/mm. Among these devices, a superb saturation along with the maximum normalized drain current density of 550 mA/mm is observed. The subthreshold swing is about 110 mV/dec and the I_{ON}/I_{OFF} ratio is as high as 3.7×10^7.

III. ANALYSIS

Due to the substantial electric field dependence of the FN tunneling process, to correctly analyze FN tunneling at large negative values of V_{GS} as a contributor to the gate current at different drain biases, the electric field (E) established across the AlGaN barrier layer has to be accurately estimated. Employing Comsol Multiphysics [19], device simulations were conducted to realistically estimate this component of electric field across the barrier. In these simulations, source and drain contacts were considered as ideally ohmic, where rightly assuming Ni gate, the gate was defined as a Schottky contact with metal work function of 5.2 eV and Schottky barrier height of 1.07 eV. In the presented simulations, the polar-induced 2-DEG concentration was defined equal to theoretical value of 1.25×10^{13} cm^{-2} (for Al mole fraction equal to 0.25 in the $Al_xGa_{1-x}N$ barrier) [22], which is in agreement with the values reported for similar heterostructure [23-24]. The material parameters, which are reported in Table I, were appropriately

TABLE II
EXTRACTED PARAMETERS USED IN EXPRESSING THE FN TUNNELING CURRENT THROUGH THE BARRIER AT DIFFERENT DRAIN BIAS

Drain to source Voltage, V_{DS}	Slope of linear relation between $\ln(I_G/E^2)$ versus E^{-1}. Slope is presented in units of MV/cm	Magnification of E across the FN leakage zone area (γ)	S_{FN}, FN leakage zone area (m^2)
0 V	-24.2	1.969	1.13×10^{-16}
2 V	-24.4	1.955	1.08×10^{-16}
4 V	-24.3	1.959	1.14×10^{-16}
6 V	-24.4	1.952	1.87×10^{-18}
8 V	-24.4	1.951	1.64×10^{-18}
10 V	-24.4	1.957	1.44×10^{-18}

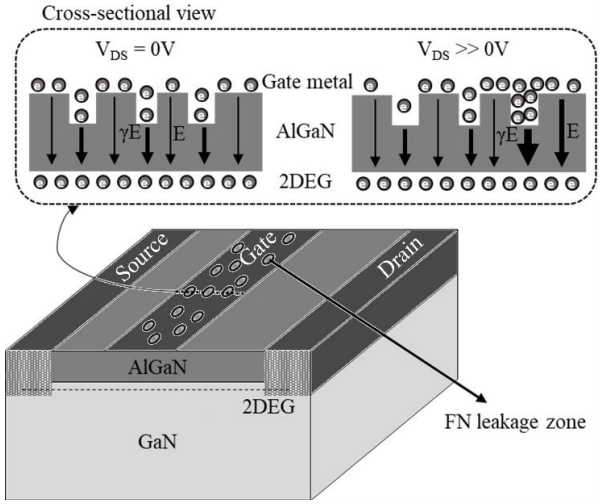

Fig 5. An illustration comparing the leakage through "FN leakage zones" at $V_{DS} = 0\,V$ and $V_{DS} >> 0V$. The size of FN leakage zones is exaggerated. The thickness of the arrows is taken to represent the strength of *E*.

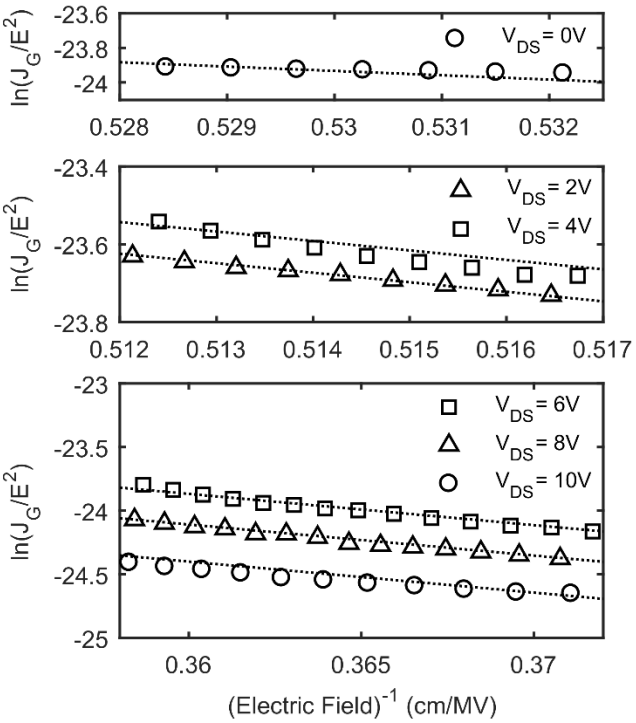

Fig. 6. Linear trend between ln (I_G/E^2) and E^{-1} at different values of V_{DS}. Symbols represent the experimentally acquired data points and the dotted lines represent the linear interpolation among these points. *E* is taken from Fig. 3(a) for V_{DS} equal to 0, 2 and 4 V, while for V_{DS} of 6, 8, and 10 V the source is Fig. 3(b).

chosen from [1] [25-27], where a field-dependent mobility model was taken into account. The AlGaN and GaN layers were rightly considered to be unintentionally doped to the level of 1×10^{14} cm^{-3}. A sufficiently fine mesh was used below the gate and across the barrier layer to account for the sharp changes in the aforementioned component of the electric field along the gate length. The obtained drain current-voltage characteristics are found to closely follow the experimental data, thus validating the performed simulations. This validation is taken as a reassurance for the accuracy of the calculated electric field profile across the barrier.

For the relatively long gates considered in this work, in the middle of the gate these simulations closely support the validity of a triangular approximation for the shape of the potential function across the polar AlGaN barrier. Whereas the values obtained for the simulated electric field in the direction normal to the heterointerface at the center of the gate is similar to the theoretical estimation of triangular barrier approximation [6], unlike the previous reported works [5], [9], [11], the value of *E* is observed not to be uniform along the gate length. The inaccurate assumption of a constant normal electric field to the heterointerface overlooks the peak of the *E* at the gate edges. Since this peak of *E* at the drain edge of the gate becomes more significant at higher drain voltages, the inaccuracy of this assumption further harms the accurate assessment of FN process under such bias conditions. Figure 3 reports the profile of this electric field versus gate voltage, at different drain voltages. The readouts presented in this figure were taken right in the middle of the thickness of the barrier at two positions along the length of the gate electrode. As shown in Fig. 3(b), the presented electric field at drain edge of the gate does not saturate with reduction of V_{GS} beyond the pinch-off condition, whereas some level of saturation can be observed in the aerial *E* shown in Figure 3(a).

Figure 4 illustrates the profile of the electric field normal to the heterointerface calculated halfway through the AlGaN barrier, for $V_{GS} = -3\,V$ and at different drain voltages. According to this observation, the difference between *E* at the center of the gate and *E* at the drain edge of the gate is of an increasing trend with the drain bias.

Corresponding to the electric field *E* across the barrier, the FN current density is often assessed according to [8-13], [18] as:

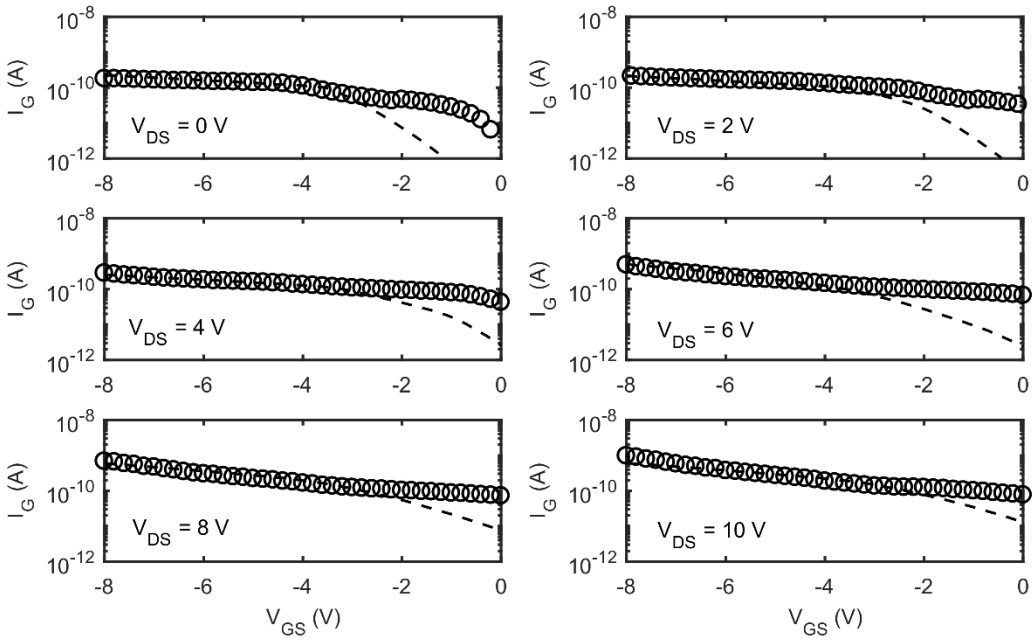

Fig. 7. I_G versus V_{GS} at different values of V_{DS}. Circles represent experimental data points. Dashed line is the calculated FN component through the AlGaN barrier (I_{FN}) discussed in section III. E is taken at the center of the gate electrode for V_{DS} equal to 0, 2, and 4, while for V_{DS} of 6, 8, and 10 V it is taken as summation of FN component of current at individual mesh nodes.

$$J_{FN} = \frac{q^2(\frac{m_e}{m_n^*})E^2}{8\pi h\phi_b}\exp\left(\frac{-B}{E}\right), \quad (1)$$

where, $$B = \frac{8\pi\sqrt{2m_n^*(q\phi_b)^3}}{3qh}, \quad (2)$$

in which, E is the electric field across the barrier layer, q is fundamental electronic charge, h is the Planck's constant, m_e is the free electron mass, m_n^* is the conduction band effective mass in the barrier layer, and $q\phi_b$ is the Schottky barrier height.

While attempts for matching the experimental gate-leakage current to the FN contribution represented by (1) often require adoption of wildly unrealistic values for m_n^* and $q\phi_b$, our previous work through temperature-dependent studies has suggested that under V_{DS} of zero volt instead of a more or less uniform FN tunneling throughout the gated area, this process is predominantly taking place through the much smaller "FN leakage zones" [11]. Whereas according to this hypothesis, presence of non-uniformity across the surface causes enhancement of E or reduction of $q\phi_b$ in these zones, without making any wild assumption about the values of m_n^* and $q\phi_b$ we have been able to accurately calculate the gate-leakage current for the aforementioned bias condition.

According to the assumption of enhanced electric field across FN leakage zones, FN contribution to gate-leakage current is expressed through a slightly modified form of (1), which is presented by

$$I_{FN} = S_{FN}\frac{q^2(\frac{m_e}{m_n^*})(\gamma E)^2}{8\pi h\phi_b}\exp\left(\frac{-B}{\gamma E}\right), \quad (3)$$

where B is given in (2), S_{FN} is the area of the FN leakage zone, and γ is the magnification of E across the FN leakage zone.

In the calculations presented in this section on the basis of the (3), the value used for the potential barrier height $q\phi_b$, corresponding to Ni/$Al_{0.25}Ga_{0.75}N$ contact and taking into account the effect of barrier lowering due to presence of image forces at the metal- barrier contact [27], [28], was rightly taken as 1.07 eV. The ratio of m_n^*/m_e was also properly selected for the $Al_{0.25}Ga_{0.75}N$ barrier to be equal to 0.4 [29]. For each value of V_{DS}, as a fitting parameter we have allowed γ to take a value corresponding to the best fit between the recorded I_G for full range of V_{DS} and the I_{FN}. In these calculations, to account for the signatures that we have observed in Figs. 3 and 4, the choice of E at a specified drain voltage for calculating FN current density according to (3) is made in association with the experimentally recorded values of gate current (I_G). At large drain biases, where as shown in Fig. 1 experimental I_G does not show saturation at higher negative values of V_{GS}, we hypothesize that E at the drain edge of the gate is behind the observed unsaturating characteristics. This is since, as shown in Fig. 3(b), E itself is observed to follow an unsaturating profile at large negative values of V_{GS}. However, at zero and small drain biases, experimental I_G is observed to take on a saturating profile, hence suggesting E at positions like the middle of the gate (where the electric field saturates with large negative values of V_{GS}) to fit the criteria. Moreover, at zero and small drain biases the difference between the E at the drain edge and in the middle of the gate is substantially less than the difference observed at large drain biases (as shown in Fig. 4). Fig. 5 presents the illustration of this hypothesis, comparing the leakage through "FN leakage zones" for small values of V_{DS} versus large V_{DS} values.

To further substantiate this hypothesis, the calculation of the integrated FN current by summing up the FN component of current at individual mesh points in the Comsol numerical simulations is carried out and the result is observed to be quite similar to the FN component of current calculated in the abovementioned fashion based on the value of the electric field at the drain edge of the gate. This observation supports the mentioned speculations on the role played by the electric field at the drain edge of the gate electrode at higher V_{DS} values.

According to this background, for the sake of a stricter level of accuracy nevertheless we calculated the FN current by summing up the FN current density at individual mesh points for larger V_{DS} values (i.e. 6, 8, and 10 V). For the smaller values of V_{DS}, E at the center of the gate as a representative of the average electric-field throughout the points associated with the gated area of the channel is taken into account.

Signaling the appropriateness of the assumption of FN tunneling as the process responsible for gate-leakage, Fig. 6 illustrates the linear dependence of $\ln(J_G/E^2)$ on $1/E$ [3], [9-12], [18]. According to (3), assuming the dominance of the FN process, the slope of this linear characteristic is proportional to $\sqrt{m_n^*(\phi_b)^3}$. For a representative device (among those referred to in Section II), Table II shows the slope of this linear characteristic at different values of drain bias. Confirming the dominance of FN tunneling, the extrapolated values of this slope while quite independent of the drain bias, are agreeing with the selected values of $q\phi_b$ and m_n^*.

What is especially interesting among the entries of Table II, is that, as anticipated the value of γ is quite independent of the drain bias, while a marked difference is observed between the required values of S_{FN} amongst the entries corresponding to the two relative groups of low and high V_{DS}. The much smaller values of S_{FN} for V_{DS} values of 6, 8, and 10, in comparison to the values necessary for this parameter when drain bias is lower, is agreeing with our earlier speculation presented in Fig. 5 that at higher drain biases only a much smaller portion of the gated barrier (located at the drain edge of the gate) is responsible for FN tunneling. We tend to believe this substantial change in S_{FN} to be due to higher nonuniformity of electric field profile along the gated length of the channel when V_{DS} is higher. For multiple V_{DS} values, Fig. 7 demonstrates the superb matching between the modeled FN induced leakage current and the measured gate leakage current for V_{GS} smaller than the threshold voltage. For V_{GS} larger than the threshold voltage, the observed diverging amounts of gate leakage from the prediction of FN tunneling mechanism, as shown by various other models [3-7], [9-13], are contributions of other leakage mechanisms such as Poole-Frenkel emission, and trap-assisted tunneling.

IV. Conclusion

Through assessing the applicability of Fowler-Nordheim tunneling mechanism of reverse gate-leakage current (previously substantiated through temperature-dependent studies) at multiple values of V_{DS}, we have succeeded in further substantiating the hypothesis of tunneling through a very limited area of the gated barrier referred to as "FN leakage zone". This assessment convincingly shows that considering such zones of tunneling, the FN component of gate-leakage can be predicted without making unrealistic assumption about the electron effective mass and the potential barrier height. Recognizing these zones and studying their root causes, can pave the way for further improving the reverse gate-leakage current of AlGaN/GaN HFETs.

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